HCMOS Design Considerations

SCLA007A

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TEXAS INSTRUMENTS

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Mailing Address:

Texas Instruments
Post Office Box 655303
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Introduction

HCMOS data sheets specify, under recommended operating conditions, input t_t = 1000 ns, (10%–90%) for V_{CC} = 2 V. If certain devices are used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Devices susceptible to the above condition are: HC112, HC161, HC163, HC164, HC165, HC166, HC191, HC193, HC393, HC590A, and HC4040.

HCMOS Designer's Information

CMOS Circuitry

The elementary CMOS building blocks are the inverter and the transmission gate. Each uses a complementary pair of one N-channel and one P-channel enhancement-type field-effect transistor. Figures 1 and 2 show these together with various logic symbols[1] used to represent them.

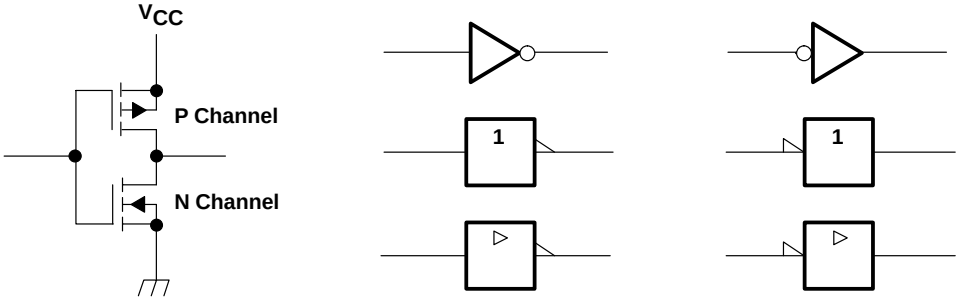


Figure 1. Inverters

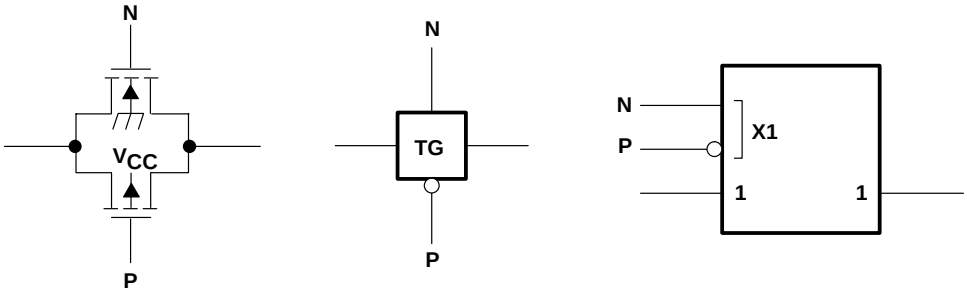


Figure 2. Transmission Gates

[1] The various logic symbols are equivalent. The distinctive-shape form of the inverter and gate symbols and the "TG" form of the transmission gate typically are used in the device logic diagrams. The logic inversion symbol (○) is shown at the input or the output, whichever maintains logical consistency with the driving output or the driven input. This technique is used to indicate the true/complement levels of the signal as it progresses through the circuit. For example, refer to Figure 7 in this section. The rectangular forms of the inverter and gate symbols and the polarity indicator (◺) replacing the inversion symbol usually are used in this book only in the device logic symbols. The ▷ indicates a high-current output.

Logic gates are created by adding transistors in parallel or in series to the transistors making up the elementary inverter. Thus, the simplest gates are inverting (see Figure 3). An odd number of additional inverters is sometimes added to the outputs of gates to make them noninverting. Basic CMOS gates usually have no more than three inputs. Arrays of gates are used when more than three signals are ANDed or ORed.

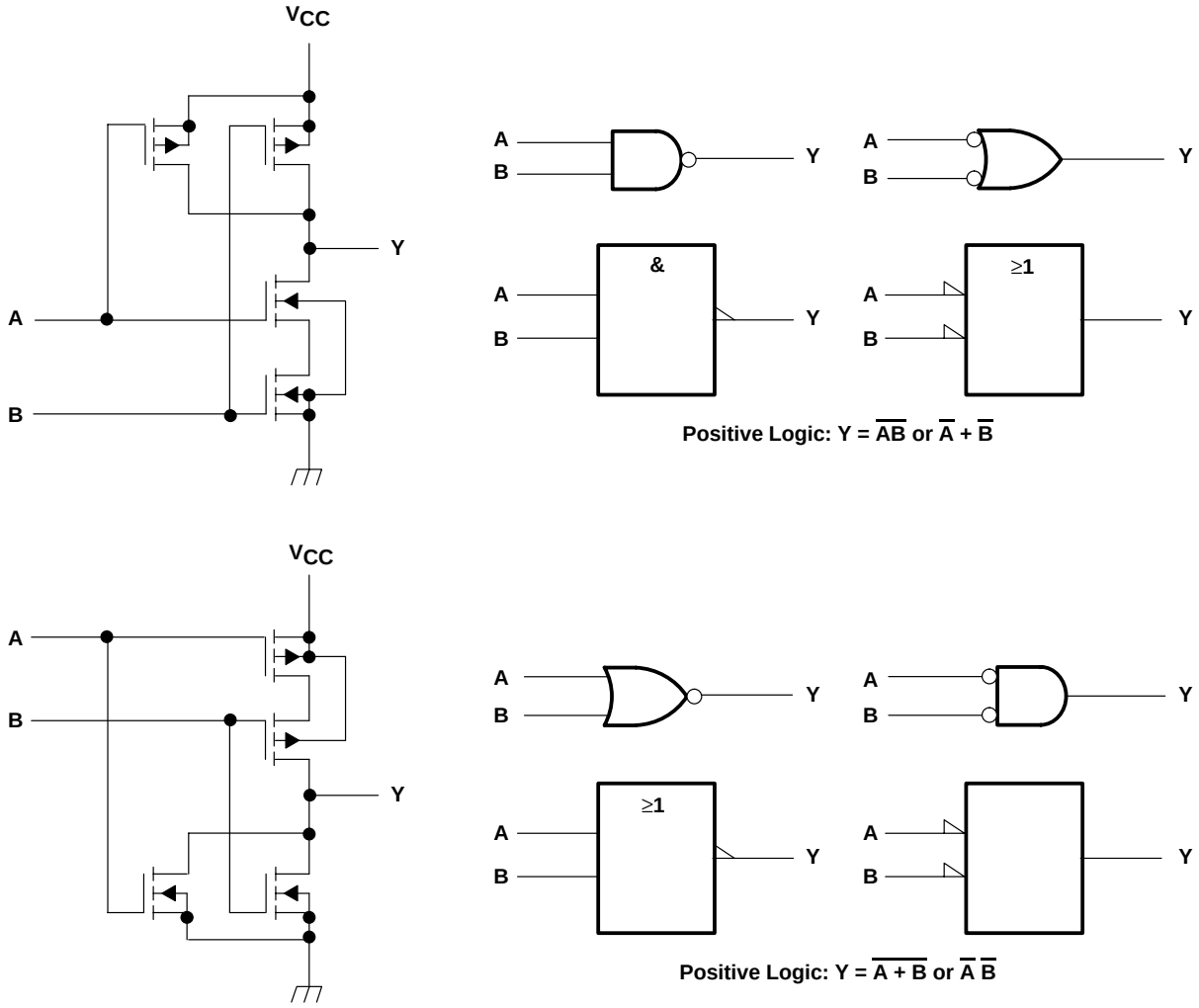


Figure 3. Gates

The exclusive-OR or exclusive-NOR gate is implemented most easily using two inverters and two transmission gates as shown in Figure 4. In complex chains of gates, the inverters can be made unnecessary by complementary signals that are already available.

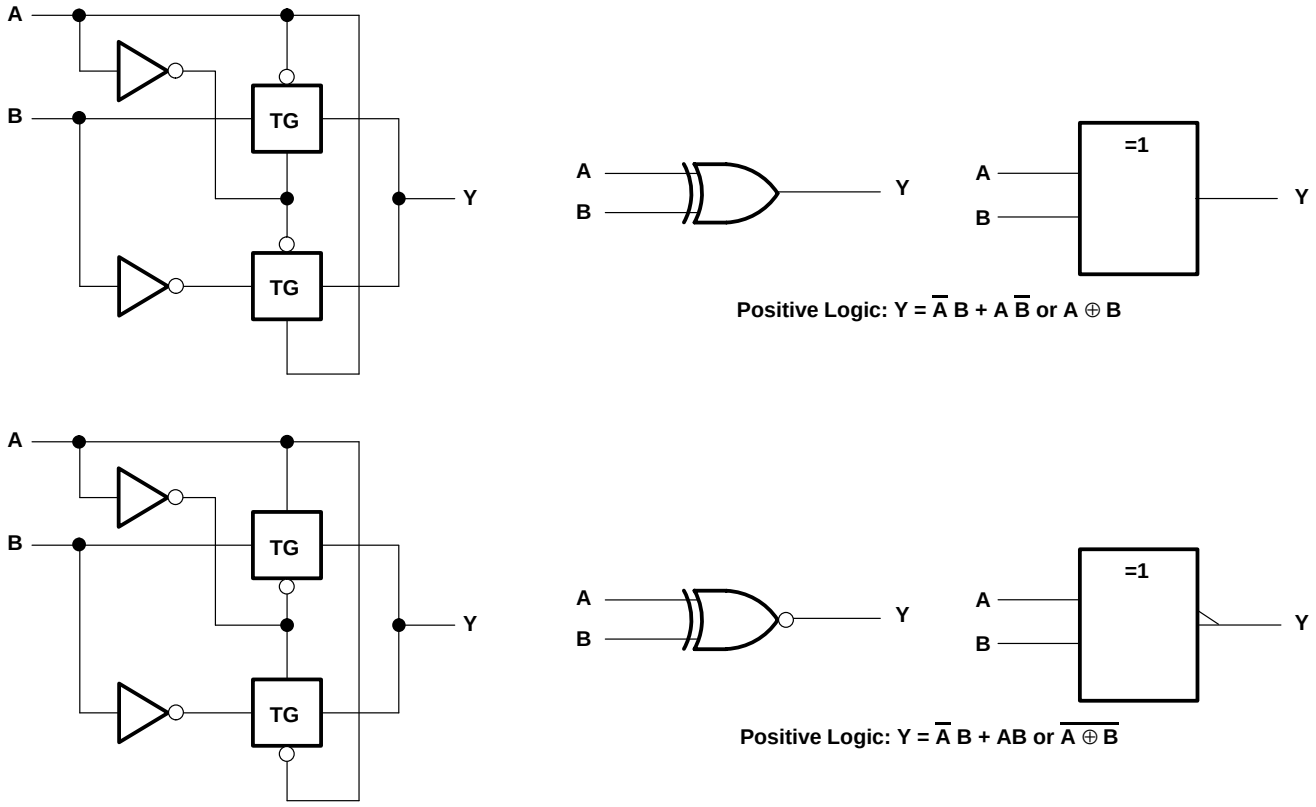


Figure 4. Exclusive-OR/NOR Gates

The 3-state output buffer has logic elements in the gate connections to each of the transistors in the final inverter so that both can be turned off under the control of an enable function. Figure 5 illustrates an inverting output buffer.

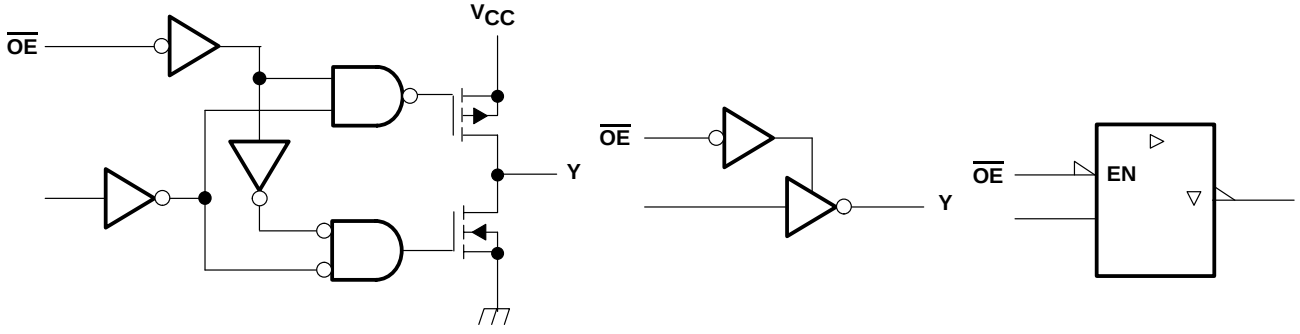


Figure 5. Inverting 3-State Output Buffer With Active-Low Enable

The transparent latch typically is implemented as shown in Figure 6. This is the simplest form. Logic diagrams show that additional inverters can be added as buffers or to optimize timing. The true and complementary outputs (Q and $\overline{Q}$) may be taken off at other points. Outputs brought out to terminals always are buffered to minimize any feedback effects. The exception to this is the HCU device, which has unbuffered outputs.

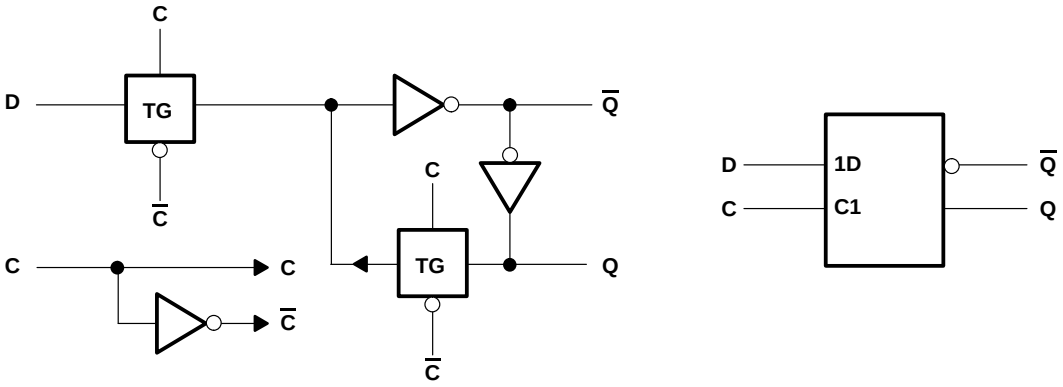


Figure 6. Transparent Latches

Putting two transparent latches in series produces an edge-triggered D-type flip-flop. Inverters can be converted to 2-input gates to provide asynchronous set and reset functions. Figure 7 illustrates a negative-edge-triggered circuit. Exchanging the connections of C and $\overline{C}$ produces a positive-edge-triggered version.

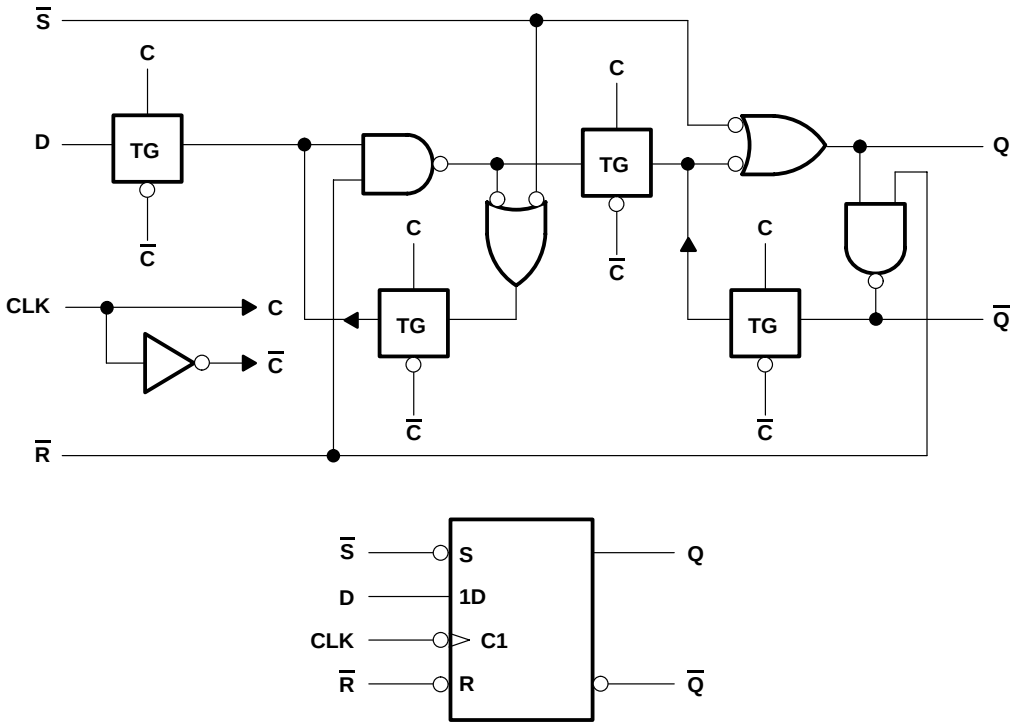


Figure 7. Negative-Edge-Triggered D-Type Flip-Flops

Detailed logic diagrams for flip-flops are given in the data sheets, when useful, to illustrate special features, such as synchronous clearing, J/K inputs, and toggle enabling.

In general, the logic diagrams have been simplified. They indicate the logic implementation, but should not be used to predict dynamic performance. Inverters existing in series can be combined or eliminated in the diagrams, as shown in Figure 8.

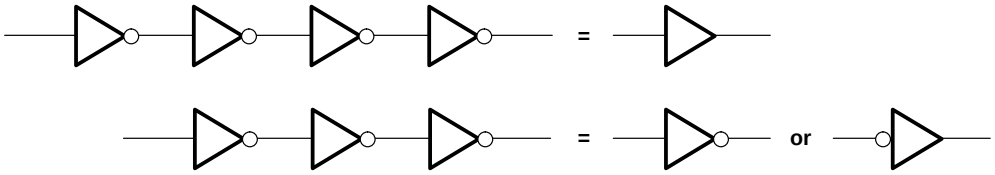


Figure 8. Simplification of Diagrams by Combining Inverters

High-Speed CMOS Characteristics

Table 1 compares the main characteristics of the high-speed CMOS family with those of standard TTL, LS, S, ALS, AS, and metal-gate CMOS.

Table 1. Performance Comparison of High-Speed CMOS With Several Other Logic Families

TECHNOLOGY†	SILICON-GATE CMOS	AHC	METAL-GATE CMOS	STD TTL	LOW-POWER SCHOTTKY TTL	ADVANCED LOW-POWER SCHOTTKY TTL	ADVANCED SCHOTTKY TTL
Device series	SN74HC		4000	SN74	SN74LS	SN74ALS	SN74AS
Power dissipation per gate (mW)							
Static	0.0000025	0.00009	0.001	10	2	1	8.5
At 100 kHz	0.17	0.006	0.1	10	2	1	8.5
Propagation delay time (ns) (C_L = 15 pF)	8	3.7	105	10	10	4	1.5
Maximum clock frequency (MHz) (C_L = 15 pF)	40	130	12	35	40	70	200
Minimum output drive (mA) (V_O = 0.4 V)							
Standard outputs	4	8	1.6	16	8	8	20
High-current outputs	6	8	1.6	48	24	24/48	48/64
Fan-out (LS loads)							
Standard outputs	10	20	4	40	20	20	50
High-current outputs	15	20	4	120	60	60/120	120/160
Maximum input current, I_{IL} (mA) (V_I = 0.4 V)	±0.001	±0.001	–0.001	–1.6	–0.4	–0.1	–0.5

† Family characteristics at 25°C, V_{CC} = 5 V; all values typical unless otherwise noted. This table is provided for broad comparisons only. Parameters for specific devices within a family may vary. For detailed comparisons, please consult the appropriate data book.

The major advantages of high-speed CMOS can be summarized as follows:

- The high-speed CMOS family can operate at speeds comparable to LS. The high-speed CMOS family has ac parameters ensured at a supply voltage of 2 V, 4.5 V, and 6 V over the full operating temperature range into a 50-pF load (also, 150 pF for high-current outputs). Note that at the higher operating frequencies, the power consumption also is comparable to LS (see Figure 9).
- Figure 9 also shows that the high-speed CMOS family covers a wide range of applications: low-power drain for low-speed systems and a slightly higher drain for higher-speed systems.

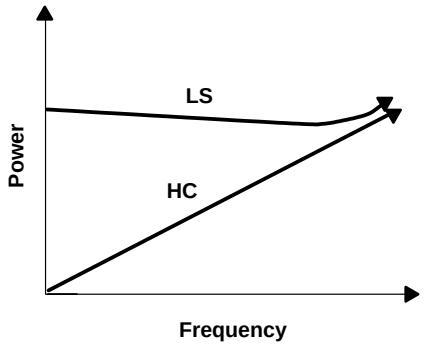


Figure 9. Power Consumed vs Frequency for High-Speed CMOS Compared to LS

- Minimum system power. Only the gates that are switching contribute to system power consumption. This reduces the size of the power supply required, resulting in lower system cost and improved reliability through lower heat dissipation.

  As mentioned previously, the power consumption for an individual gate at the maximum speed is comparable to LS. However, in typical systems, only a fraction of the gates are switching at the clock frequency; therefore, significant power savings can be realized. On a system level where the individual gate switching frequencies are distributed between zero and the system clock frequency (see Figure 10), the power saved with high-speed CMOS can be quite significant, as shown in Figure 11. The total system power is the area under each curve. The graph in Figure 11 is obtained by multiplying the individual gate characteristics (see Figure 9) by the frequency distribution in Figure 10.

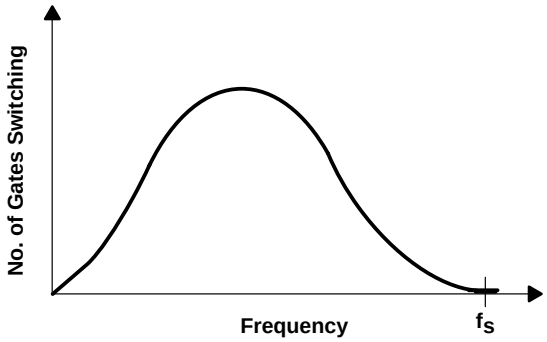


Figure 10. Typical Distribution of Switching Frequencies for Gates Within a System With Maximum Clock Frequency, f_S

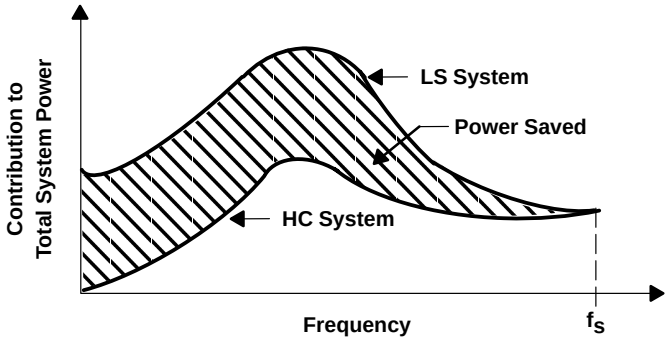


Figure 11. Contribution to Total Power by Gates Running at Frequencies From 0 to f_S

- High-speed CMOS is ideal for battery-operated systems or systems requiring battery backup because there is virtually no static power dissipation (see Figure 9).
- Improved noise immunity over bipolar devices is due to the rail-to-rail (V_{CC} to ground) output voltage swings. Figure 12 illustrates the noise immunity provided by the high-speed CMOS family as it compares to the LS family. This noise immunity makes it ideal for high-noise environments. Minimum and maximum output voltages are ensured at 4 mA (6 mA for high-current devices). If the output currents exceed these limits, the noise immunity is impaired. HCT devices have input noise margins similar to LS because their inputs are TTL-voltage compatible. The outputs of HCT are the same as standard HC outputs.

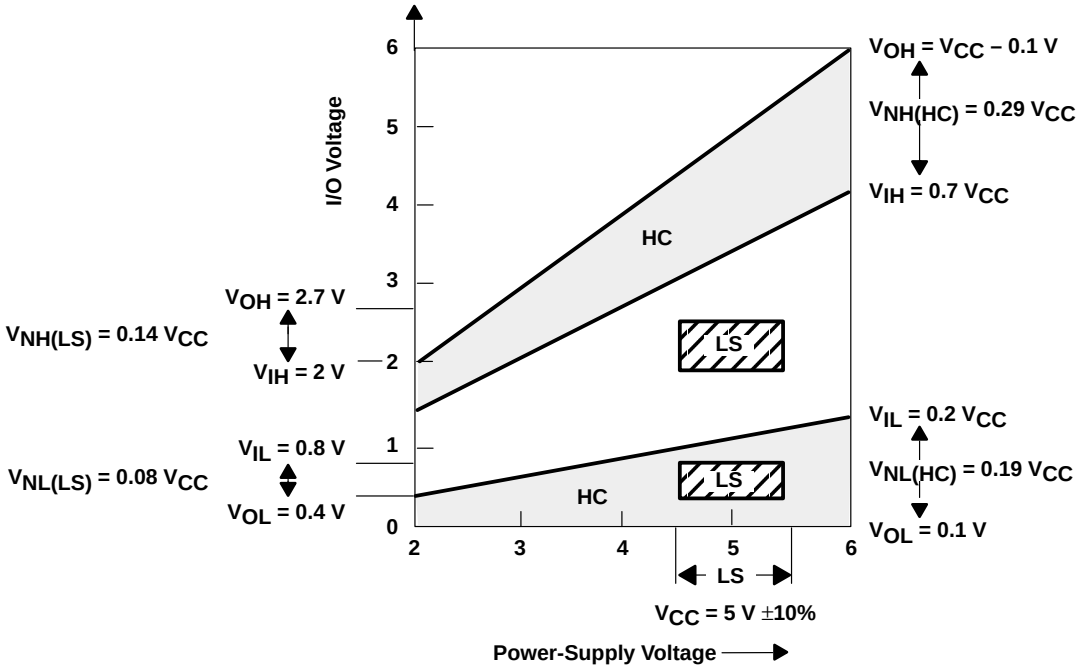


Figure 12. High-Speed CMOS and LS Noise Margins

- High-speed CMOS devices can drive up to 10 LS loads (15 LS loads for high-current outputs) while maintaining good noise immunity.
- High-speed CMOS devices are specified for operation over an extended temperature range:

  SN54HC/HCT –55°C to 125°C (military)

  SN74HC/HCT –40°C to 85°C (industrial)

All specified ac and dc characteristics are ensured over this range with the exception of power dissipation capacitance (C_{pd}), which is specified as a typical value at 25°C.

Protection Circuitry

Electrostatic discharge (ESD) and latch-up are two traditional causes of CMOS device failure. To protect HCMOS devices from ESD and latch-up, additional circuitry has been implemented on the inputs and outputs.

ESD Protection

ESD occurs when a buildup of static charges on one surface arcs through a dielectric to another surface that has the opposite charge. If this discharge current flows through an integrated circuit, the high currents can damage delicate devices on the chip. The protection circuits designed by Texas Instruments (TI) operate by shunting any excessive current safely around the sensitive circuitry on the chip. This provides ESD immunity on inputs and outputs that exceeds MIL-STD-883B, Method 3015 requirements for ESD protection (2000 V, 1500 Ω, and 100 pF).

There are two types of input protection used in HCMOS, depending on device type. Figures 13a and 13b show the two input protection circuits. Both contain diodes that are forward biased for input voltages greater than V_{CC} + 0.5 V.

In Figure 13a, the two transistors and resistor are merged into a single geometry. The transistor is distributed along the length of the resistor to clamp negative-going transients.

In Figure 13b, the main protection is provided by a low-voltage-triggered SCR (LVTSCR), which fires for positive-going transients and acts as diode to ground for negative-going transients. The MOS devices shown are located at the gates of the input circuitry and provide further clamping.

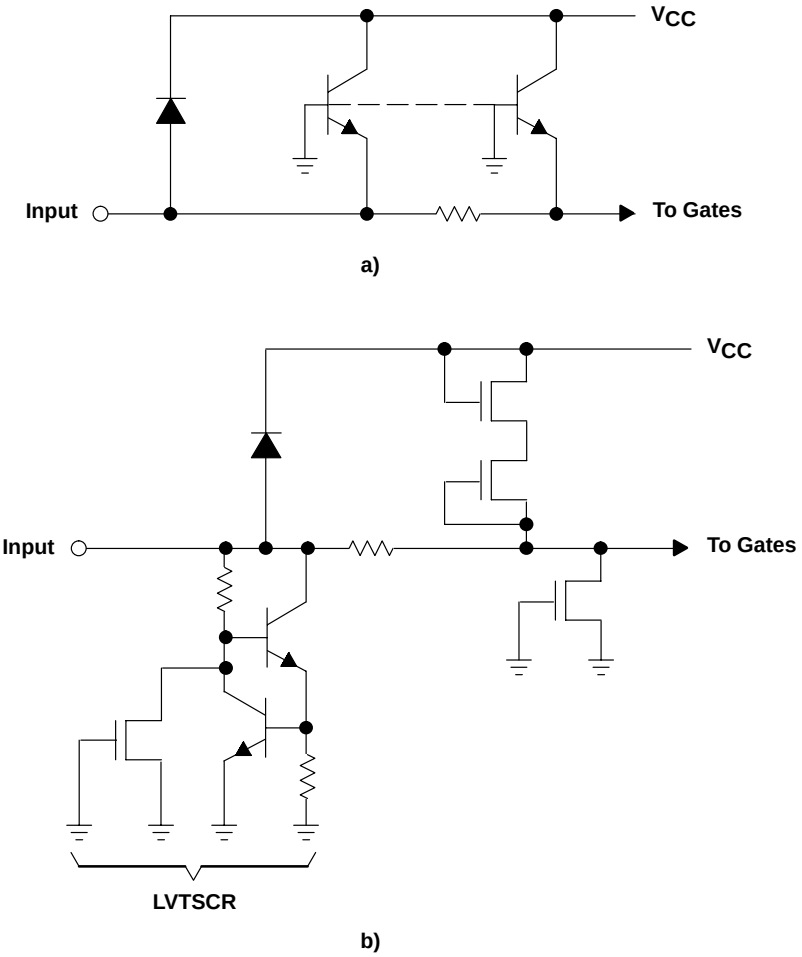


Figure 13. ESD Input Protection Circuitry

There are two types of output protection used, depending on device type. Both include a parasitic diode (D1) that clamps the voltage to within 0.5 V of the power-supply rails.

In Figure 14a, an additional diode (D2) is used to augment the parasitic diode. In Figure 14b, an LVTSCR is used to provide additional clamping.

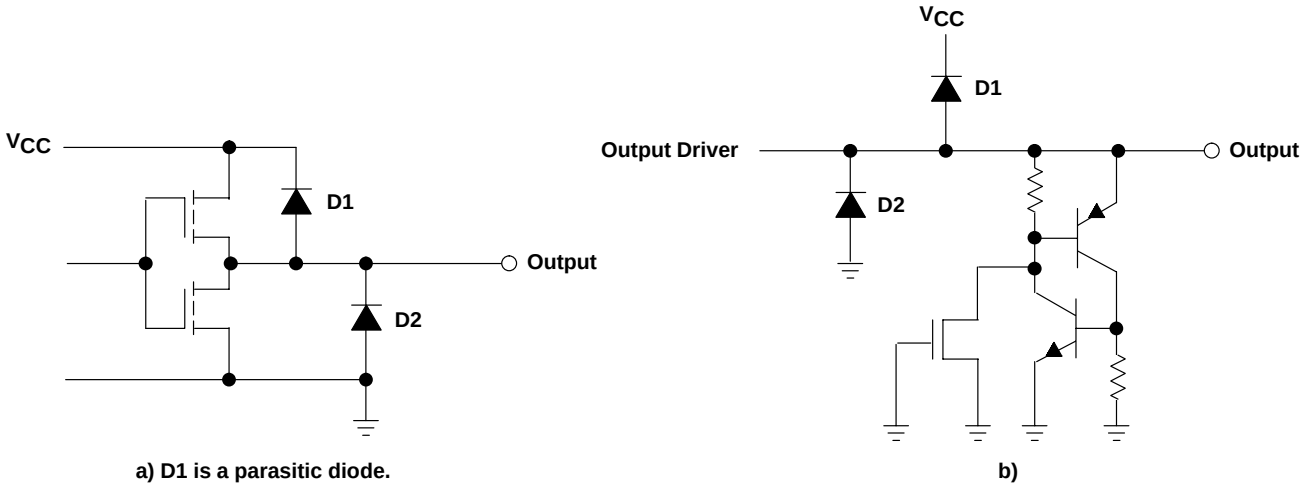


Figure 14. ESD Output Protection Circuitry

Latch-Up Protection

Latch-up cannot be completely eliminated. The alternative is to impede the triggering of the thyristor. Additional diffusions called guard rings are used to collect trigger currents before they can reach the junctions of the thyristor.

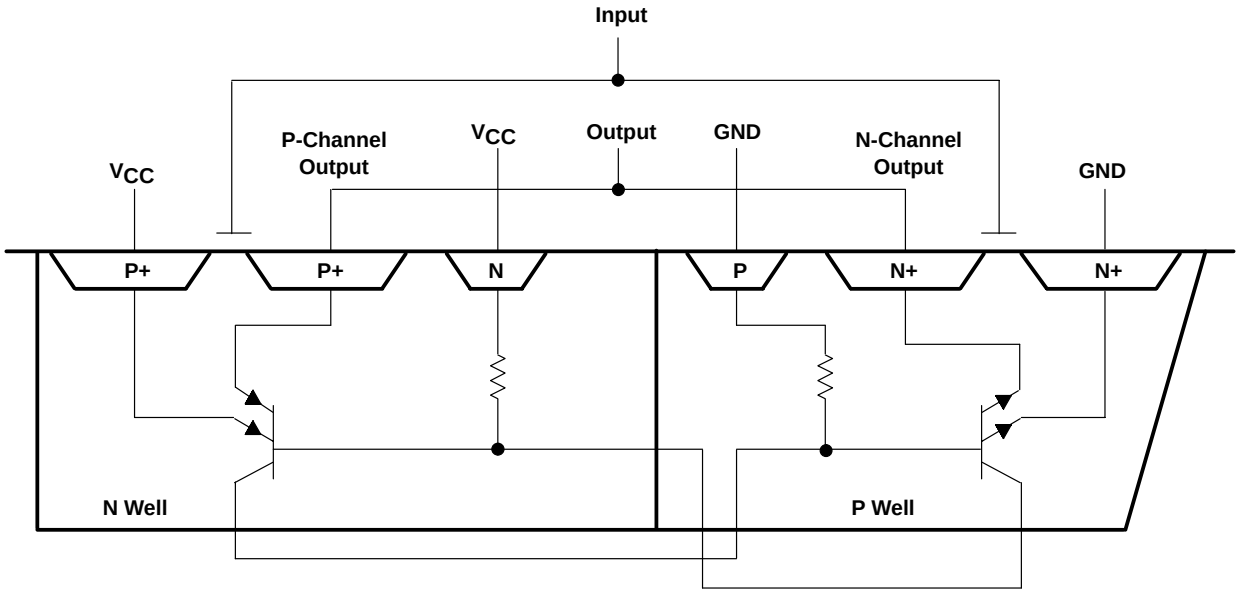


Figure 15. Parasitic Bipolar Transistors in CMOS

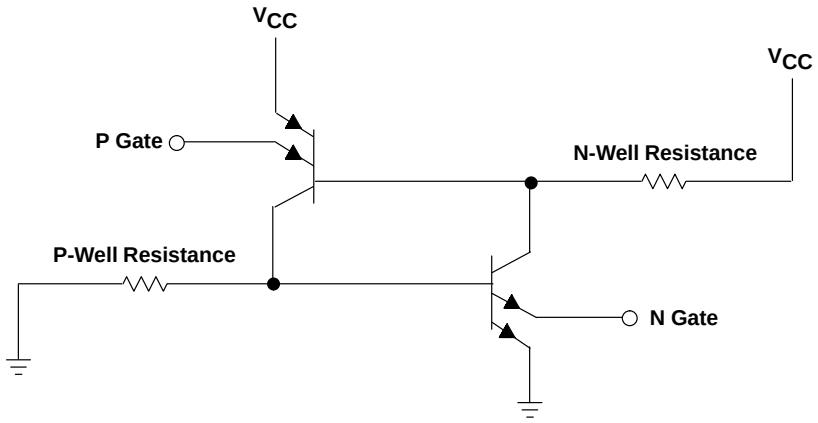


Figure 16. Schematic of Parasitic SCR With P-Gate and N-Gate Electrodes Connected

Two guard-ringing schemes are used, depending on device type. In one, any diffusion that is connected to a package pin is surrounded by four guard rings alternately connected to V_{CC} and ground, as shown in Figure 17. These guard rings collect any currents that can be injected into the substrate by signals on the device pins. Internal p-n junctions are separated by two guard rings.

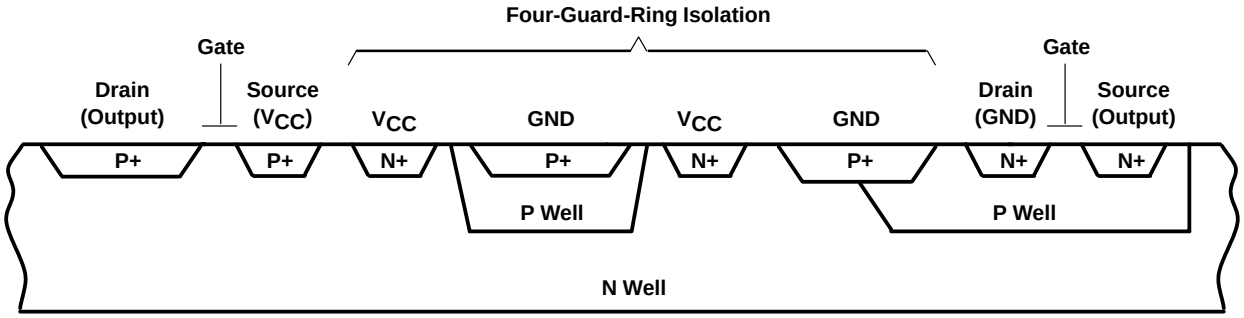


Figure 17. Unique Latch-Up Suppression Utilizes Guard Rings to Virtually Eliminate Latch-Up

In the second guard-ring scheme, any diffusion that is connected to a package pin is surrounded by a grounded p-type guard ring. Internal p-n junctions do not have a guard ring.

Tests have shown effective latch-up protection typically greater than 250 mA at 125°C, and higher at 25°C.

Fan-Out and Capacitance Loading Effects

High-speed CMOS can support up to 10 LS loads from a single standard output, or 15 loads from a high-current output. From the dc values in the individual data sheets, the fan-out of high-speed CMOS devices is unlimited for all practical purposes. However, from an ac point of view, there is a definite limit to the fan-out. The limiting constraint is the input rise time.

With a worst-case model, about 15 pF of capacitance is associated with the input of a high-speed CMOS device (10 pF from the device itself, plus 5 pF of stray capacitance; typically, the input capacitance is 3 pF for all devices except the transceivers, which are 6 pF). The input resistance, r_i, and the output resistance, r_o, can be approximated with the following equations using the information contained in the electrical characteristics chart of the device.

$$r_i = \frac{V_I}{I_I} \quad \textbf{(1)}$$

where:

$V_I = V_{CC} = 6$ V
$I_I = 0.1$ nA

$$r_o = \frac{V_{CC} - V_{OH}}{I_{OH}} \quad \textbf{(2)}$$

where:

$V_{CC} = 4.5$ V
$V_{OH} = 4.3$ V (typical)
$I_{OH} = 4$ mA

The calculated input resistance is about 60 MΩ and the maximum output resistance is approximately 50 Ω. Figure 18 shows the schematic of the output and the input models using the values previously determined.

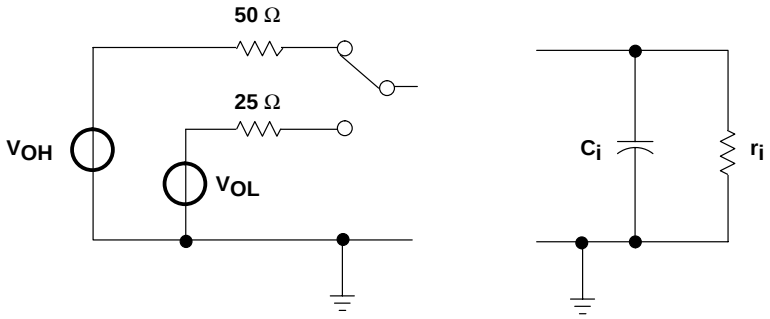


Figure 18. Worst-Case Output and Input Circuits of High-Speed CMOS

For a fan-out of n high-speed CMOS devices, the input capacitance is (n × 15) pF (capacitances are in parallel). When the driving device switches its output from the low level to the high level, the input capacitance of all devices in the fan-out must be charged up and reach V_{IH}min within 500 ns (the recommended rise time). Therefore,

$$V_{IH}\text{min} = V_{OH}\text{typ}\left(1 - e^{-t/RC}\right) \quad \textbf{(3)}$$

where:

R = 50 Ω
C = (15 × n) pF
t = 500 ns
n = number of devices in the fan-out

Taking the natural log of both sides:

$$\frac{-t}{RC} = \ln\left(1 - \frac{V_{IH}min}{V_{OH}typ}\right) \quad \textbf{(4)}$$

Substituting the appropriate values and solving for n indicates that the maximum fan-out of high-speed CMOS devices is approximately 505. Solving for t in terms of n shows that each high-speed CMOS device added to the fan-out increases the propagation delay from the input of the driving device to the input of the driven devices by about 0.989 ns. This corresponds to an added delay of approximately 0.066 ns/pF . Table 2 contains typical values of fan-out and capacitive loading effects at different values of V_{CC}.

Table 2. Typical Fan-Out of High-Speed CMOS Devices and Propagation Delay Per pF at Various Values of V_{CC}

V_{CC} (V)	V_{OH}min (V)	V_{IH}min (V)	n	t_{pd}/pF (ns)
2	1.9	1.4	936	0.0667
4.5	4.4	3.15	993	0.0629
6	5.9	4.2	1004	0.0623

$$n = \frac{\frac{-t}{RC}}{\ln\left(1 - \frac{V_{IH}min}{V_{OH}min}\right)} \quad \textbf{(5)}$$

where:

R = 50 Ω
C = 8 pF
n = number of devices in the fan-out

$$\frac{t_{pd}}{pF} = \frac{500\ ns}{n \times 8\ pF} \quad \textbf{(6)}$$

Power Dissipation

The total power dissipation of high-speed CMOS devices is the sum of three components: quiescent power dissipation, P_Q; dynamic power, P_T; and capacitive power dissipation, P_C.

The quiescent power is the product of V_{CC} and the quiescent current, I_{CC}. The quiescent current is the reverse current through the diodes that are reverse biased. This reverse current generally is very small (a few nA), which makes the quiescent power almost insignificant. However, for circuits that are in static conditions for long periods of time, the quiescent power becomes a factor to be considered.

The dynamic power is due to the current that flows only when the transistors are switching from one logic level to the other. During this time, both transistors are partially on (one turning off, the other turning on), which produces a low-impedance path between V_{CC} and ground and results in a current spike. The rise (and fall) time of the input signal has a direct effect on the duration of the current spike. This is because the faster the input signal goes through the transition region, the less time both transistors are partially on. The transient power is dependent on the characteristics of the transistors, the switching frequency, and the rise time of the input signal. This component can be calculated using the following equation:

$$P_T = C_{pd} \times V_{CC}^2 \times f_i \quad \textbf{(7)}$$

where:

C_{pd} = power dissipation capacitance (specified on each data sheet)
V_{CC} = supply voltage
f_i = input signal frequency

Additional capacitive power dissipation is caused by the charging and discharging of the external load capacitance and is dependent on the switching frequency. To calculate this power, the following equation can be used:

$$P_C = C_L \times V_{CC}^2 \times f_i \quad \textbf{(8)}$$

where:

C_{pd} = power dissipation capacitance (specified on each data sheet)
V_{CC} = supply voltage
f_i = input signal frequency

$$P_C = C_L \times V_{CC}^2 \times f_o \quad \textbf{(9)}$$

where:

C_L = external (load) capacitance
V_{CC} = supply voltage
f_o = output signal frequency

HCT Power Dissipation

HCT devices are used primarily to interface TTL output signals to high-speed CMOS inputs. To make the inputs of the HCT devices TTL-voltage compatible, the input transistor geometries were changed. This increased the power consumption compared to the equivalent HC device; however, HCT still provides a considerable savings in power over TTL. The increase in power consumption results from the TTL input levels causing both transistors in the transistor pair to be partially turned on. Included in the electrical characteristics table for HCT devices is a parameter, ΔI_{CC}, that enables the designer to compute how much additional current the HCT device draws per input when at a TTL voltage level.

Power-Supply Decoupling

When an SN54/74HC gate switches, there is a brief period (about a nanosecond) during which both transistors in the gate output buffer (see Figure 19) are partially on. In this interval, the device draws a substantial supply current, producing a current spike on the V_{CC} and ground leads to the gate. This spike can exhibit di/dt as high as 5000 A/s. These spikes react with the distributed inductance of the supply wiring to produce significant voltage transients on V_{CC} and ground unless adequate supply decoupling is provided. These transients, if allowed, couple directly into the gate outputs, which in normal usage switch from rail to rail.

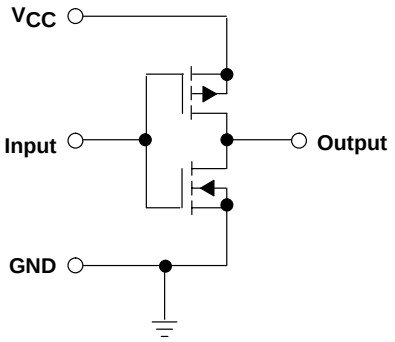


Figure 19. Gate Output Buffer

Decoupling Procedure

Figure 20 shows a circuit for testing the effectiveness of decoupling. In this test circuit, the V_{CC} and ground connections consist of two parallel runs of one-eighth-inch copper on a G-10 epoxy-glass circuit board. As a 0.01-μF decoupling capacitor between V_{CC} and ground physically is moved away from a driven gate in 1.5-inch increments, V_{CC} transients increase, as shown in Figure 21.

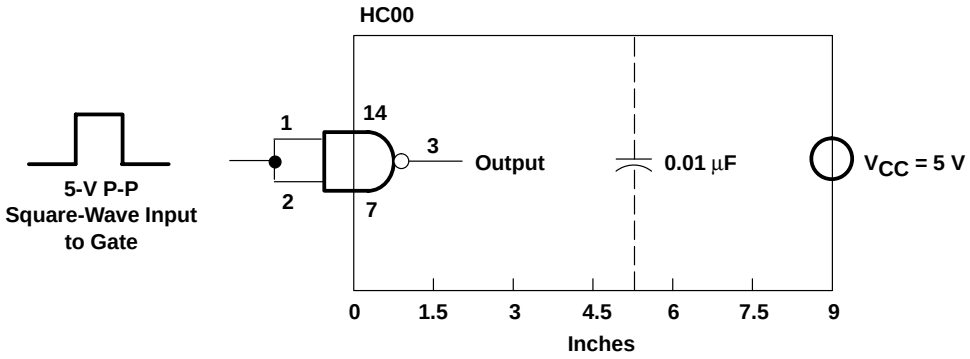


Figure 20. Test Circuit for Decoupling Effects

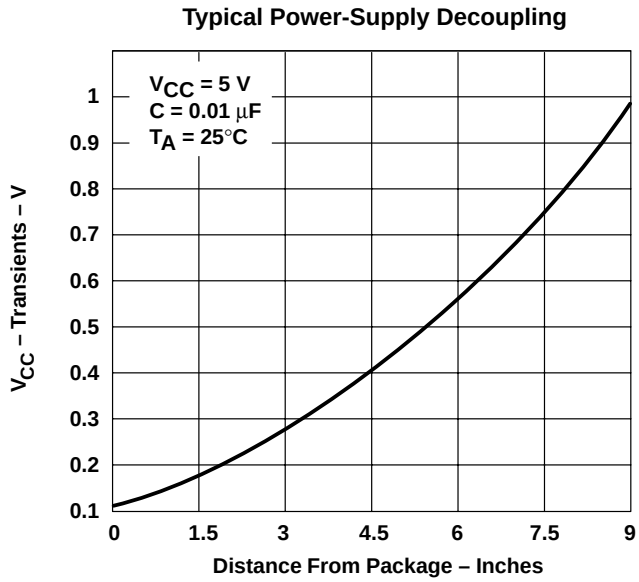


Figure 21. V_{CC} Transients vs Decoupling Capacitor Distance From DIP

The results indicate the importance of adequate decoupling and illustrate the correct procedure for obtaining it. This procedure consists of locating decoupling capacitors as close as possible to the integrated-circuit package to maximize noise margins.

Connecting Unused Inputs

Unused inputs should be tied to V_{CC} or ground to prevent the input from floating. If left to float, the power consumption of the device increases because the input may be at an invalid logic level (between V_{IH} and V_{IL}), causing I_{CC} to increase.

Matching

Another factor to consider when designing with high-speed CMOS is the V_{OH}min-to-V_I matching. This is important when the V_{OH}min of the driving device exceeds the V_{CC} + 0.5 V of the driven device. If this occurs, the ESD protection diode on the inputs is forward biased. At this point, the driving device attempts to power up the driven device's power supply. No damage occurs to the driven device if the current flowing through the diode does not exceed 20 mA.

Powering-Up/Down Sequence for High-Speed CMOS

To avoid possible damage and reliability problems with the high-speed CMOS devices when applying power, the following steps should be followed:

1. Connect ground
2. Connect V_{CC}
3. Connect the input signal

When powering down a high-speed CMOS device, follow the above steps in reverse order.

High-Speed CMOS Interfacing

Introduction

The high-speed CMOS logic family from TI contains a broad spectrum of SSI/MSI functions. Within this family are TTL functions, HCT devices, HC4000 series, and an HCU device.[2] Entire CMOS systems can be implemented using this logic family. There also is a broad range of CMOS-system to non-CMOS-system interfaces that needs to be considered. The design engineer inevitably encounters these interfaces. To develop the necessary interfaces, a thorough understanding of data-sheet parameters of both systems and an organized approach are recommended. This report uses basic examples to present one possible approach to the SN54/74HC interface solution.

There are two types of interfacing that must be considered:

- Interfacing CMOS system signals to non-CMOS systems
- Interfacing non-CMOS system signals to CMOS systems

The first type requires an understanding of the CMOS output parameters and the non-CMOS input parameters, and vice versa for the second type. In both cases, a model of the inputs and outputs of both systems may be useful.

General Interfacing Solution

An interfacing problem arises when the output logic levels and/or the current requirements of the driving system (or device) are different from the input logic levels and/or the current requirements of the driven system (or device). When determining the compatibility of the systems (or devices), the most important system/device parameters are V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, and V_{OL}.

Figure 22 is the voltage transfer characteristic of a typical unloaded inverter showing the various input- and output-voltage parameters. Loading the output of the inverter lowers V_{OH} and raises V_{OL}. The electrical characteristics table in data sheets specifies minimum V_{OH} and maximum V_{OL} for various loads.

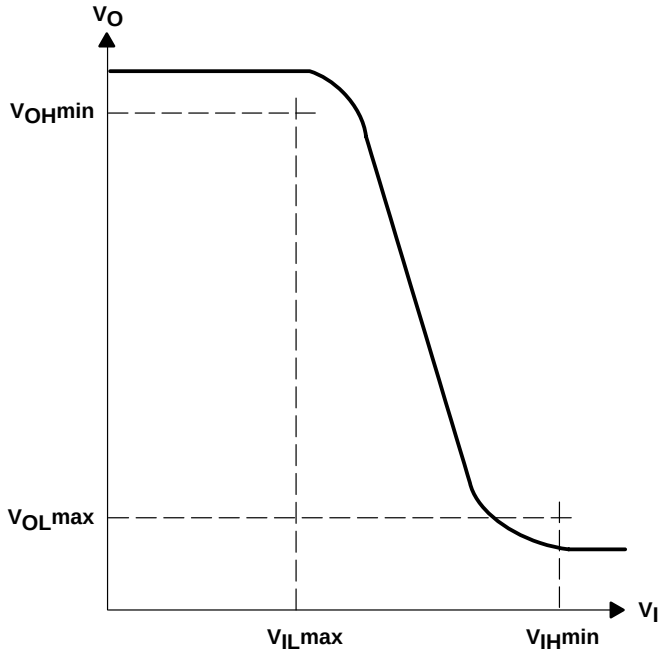


Figure 22. Voltage Transfer Characteristic of a Typical Inverter

[2] HCT devices are explained later. The HC4000 series devices are, pin-for-pin, functionally compatible, but not electrically compatible, with the older metal-gate CMOS devices. The HCU device is unbuffered.

Noise Margin

There are two noise margins to be considered: the low-voltage and the high-voltage noise margin. The voltage difference between V_{IL}max of the driven system/device and V_{OL}max of the driving system/device is the low-voltage noise margin. The voltage difference between V_{OH}min of the driving system/device and V_{IH}min of the driven system/device is the high-voltage noise margin (see Figure 23).

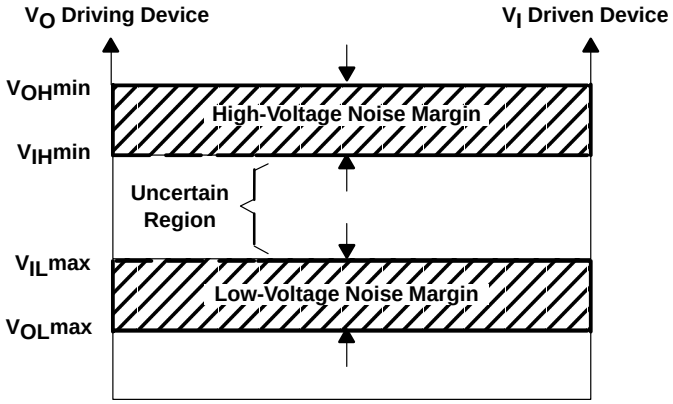


Figure 23. Noise Margins

It is desirable to have the noise margin as large as possible and the uncertain region (the difference between V_{IH}min and V_{IL}max) as small as possible. When an input voltage falls into the uncertain region, we do not know how the output, in conjunction with other inputs driven by that output, will respond. The problem with small noise margins is that any noise on the output of the driving system or device causes the signal to fall into the uncertain region and could possibly cause a bit error in the system. There are various sources of noise in digital systems. Three possible internal sources are inductive and resistive drops, capacitive coupling from another logic node, and mutual inductance with another logic node. Radio signals are possible external sources of noise.

As an aid for interfacing between the various TTL families, the eight parameters previously defined are shown in Table 3. The values are for V_{CC} = 5 V and T_A = 25°C (worst-case device parameters — the device performs at least this well). All currents are designated positive when flowing into the device.

Table 3. Worst-Case Values of Primary Interfacing Parameters

PARAMETER	74HCMOS	AHC	74TTL	74LS	74AS	74ALS
V_{IH}min	3.5 V	3.85 V	2 V	2 V	2 V	2 V
V_{IL}max	1 V	1.65 V	0.8 V	0.8 V	0.8 V	0.8 V
V_{OH}min	4.9 V	3.8 V	2.4 V	2.7 V	2.7 V	2.7 V
V_{OL}max	0.1 V	0.44 V	0.4 V	0.4 V	0.4 V	0.4 V
I_{IH}max	1 µA	1 µA	40 µA	20 µA	200 µA	20 µA
I_{IL}max	–1 µA	–1 µA	–1.6 mA	–400 µA	–2 mA	–100 µA
I_{OH}max	–4 mA	–8 mA	–400 µA	–400 µA	–2 mA	–400 µA
I_{OL}max	4 mA	8 mA	16 mA	8 mA	20 mA	4 mA

Driving-Gate Output Model

Figure 24 shows the model of a driving gate derived from the data-sheet specifications. $V_{OH(nl)}$ (nl = no load) is the high-level output voltage expected when the output gate is unloaded. $V_{OL(nl)}$ is the low-level output voltage expected when the output gate is unloaded. The values for these two voltages usually are not given on the data sheets. As a general rule for MOS devices, the output switches between the power rails $V_{OH(nl)} = V_{CC}$ and $V_{OL(nl)}$ = GND; for bipolar devices (e.g., the TTL family) $V_{OL(n1)}$ is about V_{CC}(sat) or about 0.3 V. $V_{OH(nl)}$ varies within the TTL family. Standard TTL has a $V_{OH(nl)}$ within two base-emitter drops of V_{CC}($V_{OH(nl)} = V_{CC} - 1.2$ V); LS has a $V_{OH(nl)}$) within one base-emitter drop of V_{CC}($V_{OH(nl)} = V_{CC} - 0.6$ V). The data sheets specify V_{OH}max and V_{OL}max at a nonzero I_{OH} and I_{OL}, respectively. Therefore, to calculate the approximate series resistances, the following two equations can be used:

$$R_{OH} = \frac{|V_{OH(nl)} - V_{OH}min|}{I_{OH}} \quad (10)$$

$$R_{OL} = \frac{|V_{OL(nl)} - V_{OL}max|}{I_{OL}} \quad (11)$$

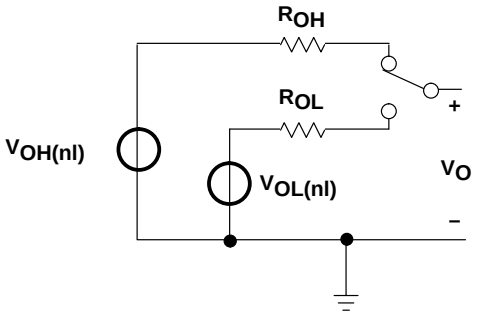


Figure 24. Output Model of a Driving Gate

Input-Gate Circuit

A simplified schematic of a high-speed CMOS input gate is shown in Figure 25. The diode (D1) and the transistors (Q1 and Q2) provide static discharge and input transient clamping for the device. Any inputs higher than V_{CC} + 0.5 V or lower than –0.5 V clamp the input. The capacitors (C1 and C2) represent the parasitic capacitances present at the gate input. The data sheet specifies that the input capacitance (C1 + C2) does not exceed 10 pF (typical is about 5 pF). The input capacitance is split between V_{CC} and ground of the device and provides a feedback path between V_{CC} and the input. If the input is driven by a high-impedance source, any transient noise on V_{CC} may be coupled back into the input.

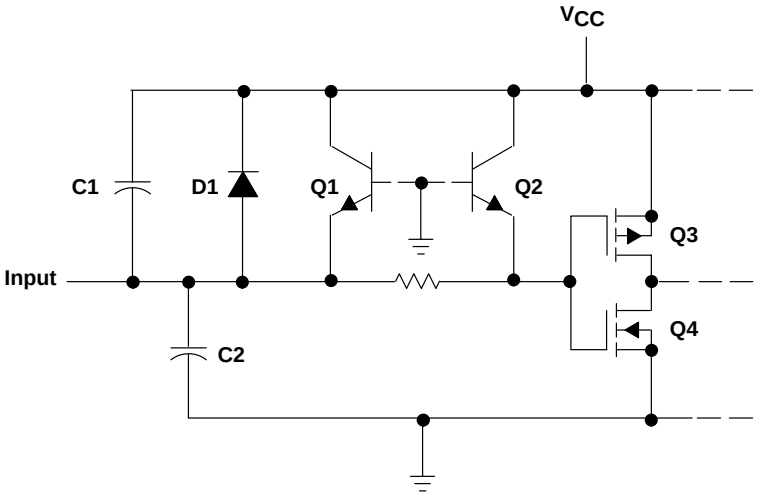


Figure 25. SN54/74HC Input Gate

CMOS-to-Standard-TTL Interface

CMOS devices can drive TTL loads with no additional interfacing required. The output voltages of CMOS devices are compatible with the input voltage requirements of TTL devices. The input current requirements of the TTL devices place a strict limitation on the number of TTL devices that CMOS devices can drive from a single output (the fan-out).

Figure 26 shows a CMOS output gate driving a TTL input gate. When the CMOS gate drives the emitter of Q3 low, a current flows into the CMOS gate from R1 and the emitter of the TTL gate. The maximum ensured current that the CMOS device can sink is 4 mA. Therefore, the maximum TTL fan-out that a device can drive without exceeding the specified limit is two (I_{IL} for TTL is –1.6 mA).

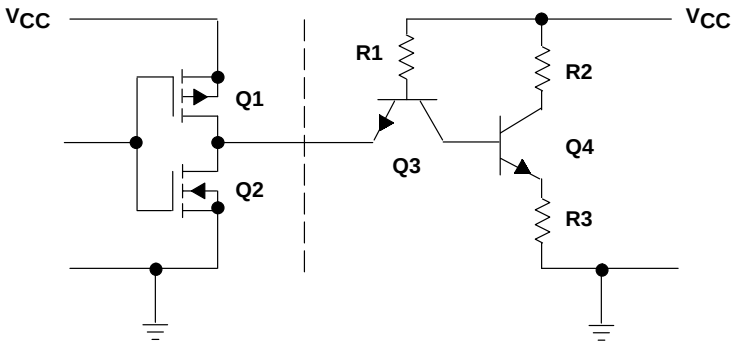


Figure 26. SN54/74HC-to-TTL Interface

Standard TTL-to-CMOS Interface

The interface for TTL driving CMOS is not as simple as the CMOS-to-standard-TTL interface. Using the voltage levels from Table 3, it is obvious that V_{OH}min of the TTL device and V_{IH}min of the CMOS device are not compatible. Figure 27 shows the schematic of the TTL-to-CMOS interface. The pullup resistor, R_p, eliminates the voltage incompatibility.

The lower limit of the pullup resistor is determined by the current-sinking capability of the driving device (TTL for this interface). When the TTL device output goes low, Q3 (see Figure 27) is required to sink a current of ($V_{CC} - V_{OL}$max)/Rp in addition to the sum of the output currents of the driven devices I_{IL} worst case. All of this is shown in the following equation:

$$R_p\,\text{min} = \frac{V_{CC} - V_{OL}\,\text{max(TTL)}}{I_{OL}\text{(TTL)} + n\ I_{IL}\text{(load)}} \quad \textbf{(12)}$$

where:

n = number of loads being driven
V_{CC} = voltage applied to the pullup resistor

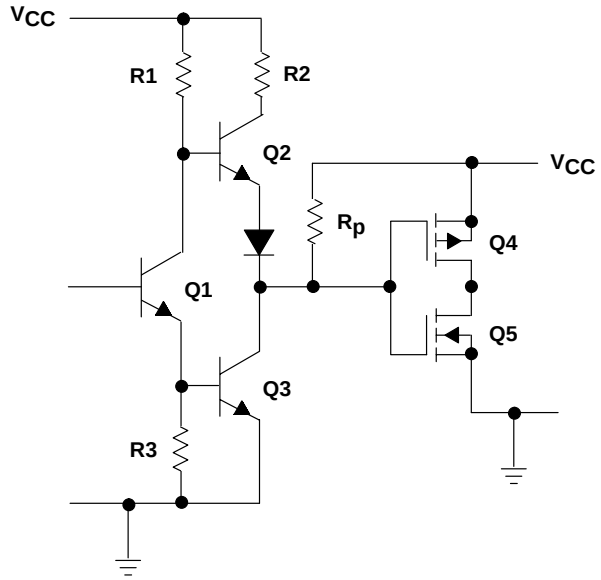


Figure 27. TTL-to-SN54/74HC Interface With a Pullup Resistor

Example 1. An SN74LS00 is driving three SN74HC00 devices.
V_{CC}min = 4.75 V, V_{OL}max = 0.4 V, I_{OL} = 8 mA, I_{IL} = 1 μA, and n = 3, therefore $R_p$min = 543 Ω.

The upper limit of the pullup resistor is determined by two factors:

- Total input capacitance of the loads
- Total high-level input currents of the loads

When the TTL output goes high, Q2 is turned off by the pullup resistor. Therefore, all the current that flows into the devices that are being driven flows through the pullup resistor, R_p. Therefore, the input voltage of the CMOS devices rises exponentially, with a time constant of R_pC_i (C_i = 10 pF max). The time constant cannot exceed the 500-ns rise-time requirement of the CMOS device. Along with this limitation, the total input currents must not cause the voltage drop across the pullup resistor to exceed V_{IH}min for the CMOS devices. The following equation can be used to determine $R_p$max:

$$R_p\,\text{max} = \frac{V_{CC} - V_{IH}\,\text{min(load)}}{|n\ I_{IH}(\text{load}) - I_{OH}(\text{driver})|} \quad \textbf{(13)}$$

where:

n = number of loads being driven
V_{CC} = voltage applied to the pullup resistor

Example 2. An SN74LS00 is driving three SN74HC00 devices.
V_{CC} = 5.25 V, V_{IH}min = 3.675 V, I_{IH} = 1 μA, I_{OH} = 0, and n = 3, therefore $R_p$max = 525 kΩ.

However, if the rise time is calculated using this value of $R_p$max, the recommended 500 ns is exceeded.

From the relationship:

$$V_{IH}\text{min} = V_{CC}\text{max}\left(1 - e^{-t/R_pC_i}\right) \quad \textbf{(14)}$$

with:

V_{IH}min = 3.675 V
V_{CC}max = 5.25 V

then:

$$R_p = \frac{t}{1.2\ C_i} = 13.8\Omega\ (t = 500\ \text{ns and}\ C_i = 30\ \text{pF}) \quad \textbf{(15)}$$

Generally, this rise-time constraint is the limiting factor on the upper limit of the pullup resistor.

CMOS-to-LS Interface

The interface of CMOS to LS is very similar to the interface of CMOS to TTL (see Figure 28). As shown, there is no pullup resistor required. When the LS input is pulled low, the current flows through R1 and D2 into the CMOS output. In the worst-case condition, this current is about 0.4 mA. Because the CMOS output parameter I_{OL} specifies a 4-mA current sink for the device, the maximum LS fan-out is ten.

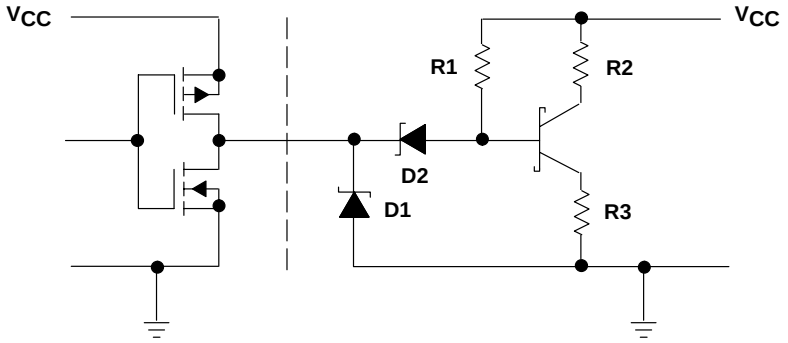


Figure 28. SN54/74HC-to-LS Interface

LS-to-CMOS Interface

For an LS device to drive a CMOS device, a pullup resistor must be used because the V_{OH}min of the LS is less than the specified V_{IH}min of the CMOS device. Figure 29 shows the schematic of the LS/CMOS interface. The upper and lower limits of the pullup resistor are determined by the same method as the TTL/CMOS interface. The upper limit of the pullup resistor is limited by the input currents and the input capacitance.

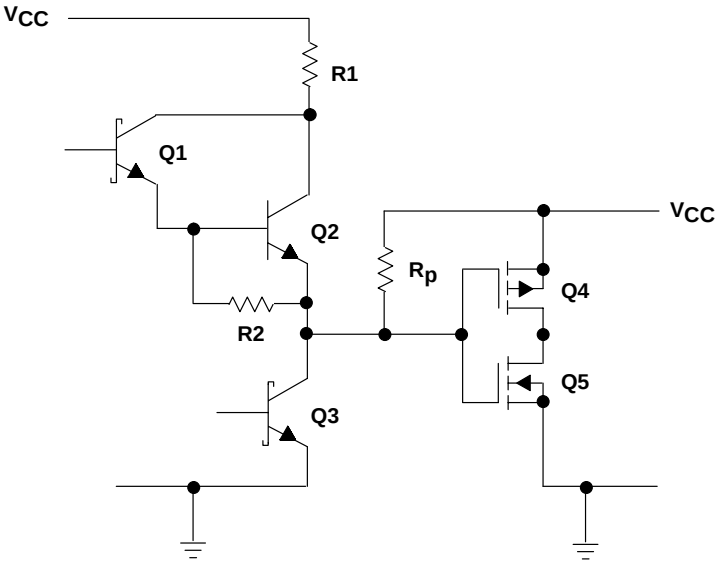


Figure 29. LS-to-SN54/74HC Interface With a Pullup Resistor

CMOS-to-ALS Interface

The output logic level of CMOS devices is completely compatible with the input logic levels of ALS devices. The interface structure with ALS is shown in Figure 30. As with the other CMOS-to-TTL interfaces, there is no pullup resistor required. The fan-out of ALS devices is determined by the amount of current that flows through Q3 into the CMOS device and the amount of current the CMOS device can sink. When the input of the ALS device is low, there is 0.1 mA flowing through Q2. The maximum current that the CMOS device can sink (according to the parameters) is 4 mA. This corresponds to an ALS fan-out of 40.

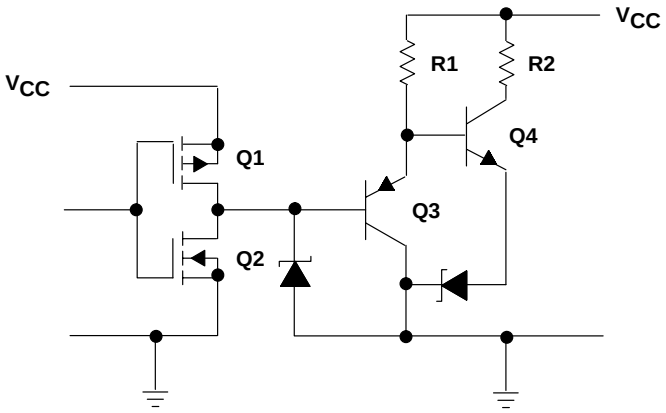


Figure 30. SN54/74HC-to-ALS Interface

ALS-to-CMOS Interface

The high-level output voltage of ALS devices is incompatible with the required high-level input voltage of CMOS devices. Because of this incompatibility, a pullup resistor is required to make the two voltage levels compatible. The method of determining the upper and lower limits of the pullup resistor is the same as the other two TTL-to-CMOS interfaces (see Figure 31).

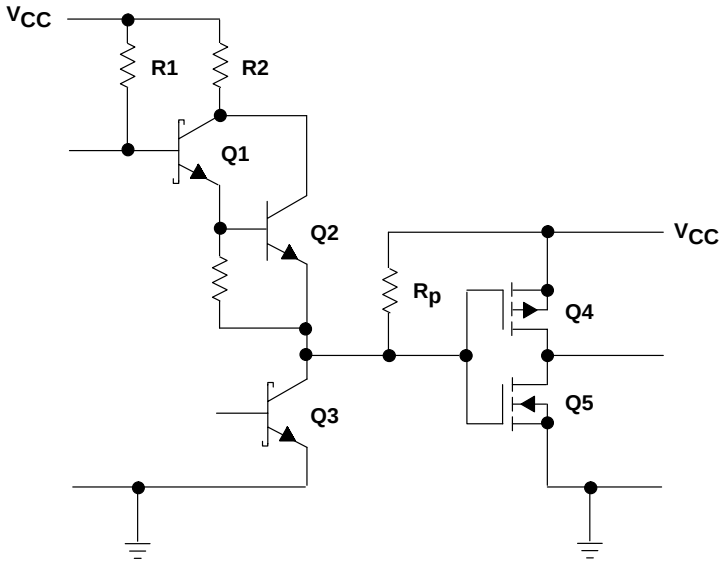


Figure 31. Interface With a Pullup Resistor

CMOS-to-AS Interface

As in the case of the other CMOS-to-TTL interfaces, no pullup resistor is required (see Figure 32) because the input voltage levels of AS are compatible with the output voltage levels of CMOS. The fan-out of AS devices is limited by the low-level input current (I_{IL}) of AS and the current-sinking capability of CMOS (I_{OL}). I_{IL} for the AS is 2 mA, and the current-sinking limit of CMOS is 4 mA. Therefore, the fan-out is two AS devices.

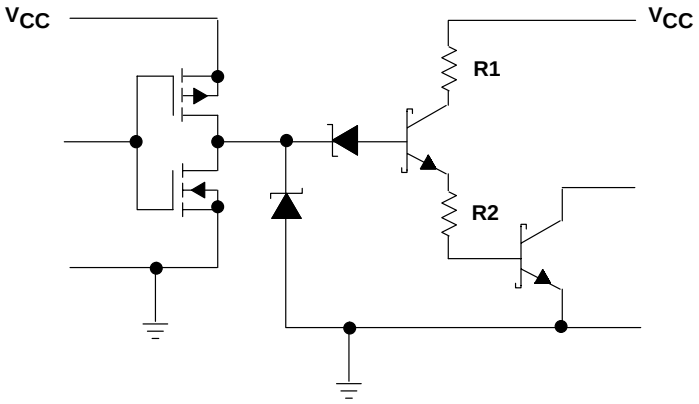


Figure 32. SN54/74HC-to-AS Interface

AS-to-CMOS Interface

Not all the output logic levels of AS are compatible with the input logic levels of CMOS. Table 4 shows there is incompatibility between the V_{OH} of AS and V_{IH} of CMOS. As with other TTL-to-CMOS interfaces, a pullup resistor is required (see Figure 33). The appropriate value of the pullup resistor is determined by the same procedure previously explained.

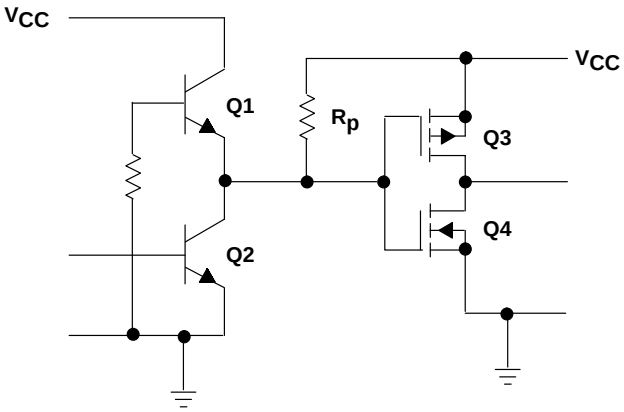


Figure 33. AS-to-SN54/74HC Interface With a Pullup Resistor

CMOS-to-NMOS Interface

NMOS is used extensively in large-scale integration products such as microprocessors, microcomputers, and memories. The logic levels of NMOS usually are TTL compatible. CMOS devices can drive NMOS devices with no pullup resistors. The input impedance of NMOS is very high, which is similar to the input impedance of CMOS.

NMOS-to-CMOS Interface

A pullup resistor may be necessary when an NMOS device drives a CMOS device. The method of determining the value range of the pullup resistor is the same as the method described previously for TTL. A quick look at NMOS output parameters and CMOS input parameters determines if a pullup resistor is required.

Using HCT Devices to Interface with CMOS From TTL

There are two methods to interface from a TTL system (standard TTL, LS, AS, ALS):

- Use of pullup resistors (as previously described)
- Use of HCT devices (by far the easier method)

The HCT device inputs are TTL compatible; the outputs are both TTL and CMOS compatible. Therefore, all the interface requires is to connect the TTL system output into the HCT device, and the output of the HCT device can then be used for the input of the CMOS system.

Oscillators

RC Oscillators

Simple oscillator circuits using a minimum number of components can be designed with high-speed CMOS devices, e.g., two HC04, HCU04, or HC02 gates. These oscillators generate a period of approximately 1.8 RC seconds (see Figure 34).

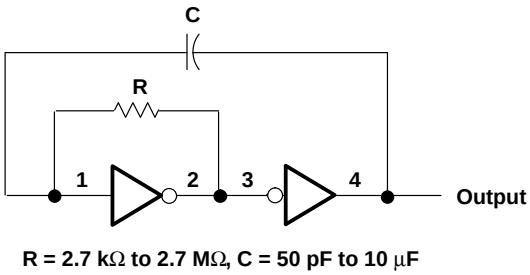


Figure 34. Simple RC Oscillator Using Two HC04 Gates

Crystal-Controlled Oscillators

A crystal or ceramic resonator can be used to set the oscillator period (see Figure 35). The value of the resistor, typically 100 kΩ, may require special selection to ensure oscillation at the desired fundamental resonator frequency. The capacitor, typically 100 pF, is required to dampen parasitic oscillations in the 30-MHz to 50-MHz range.

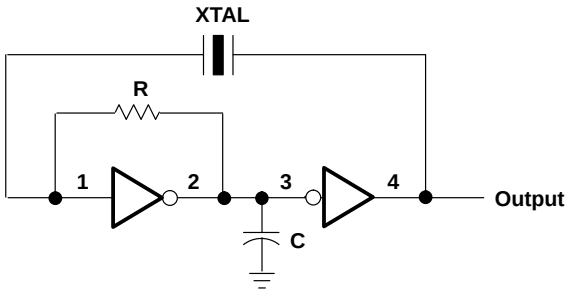


Figure 35. Oscillator Circuit Using a Crystal to Set the Period

Voltage-Controlled Oscillators

Voltage-controlled oscillators (VCOs) also can be designed using a minimal number of components. Figure 36 shows a VCO using NAND and inverter gates. This VCO design exploits the phenomena of the slight variations in the propagation delay of an HC gate with changes in the supply voltage. The HC00 is connected as a three-stage ring oscillator with a buffer. As the control (supply) voltage, V_C, is varied, the ring oscillator's frequency changes according to the following:

$$f_{out} \text{ in MHz} \approx 5.8 \times V_C \quad \textbf{(16)}$$

Where:

V_C is in the range of 1.5 V to 4.5 V.

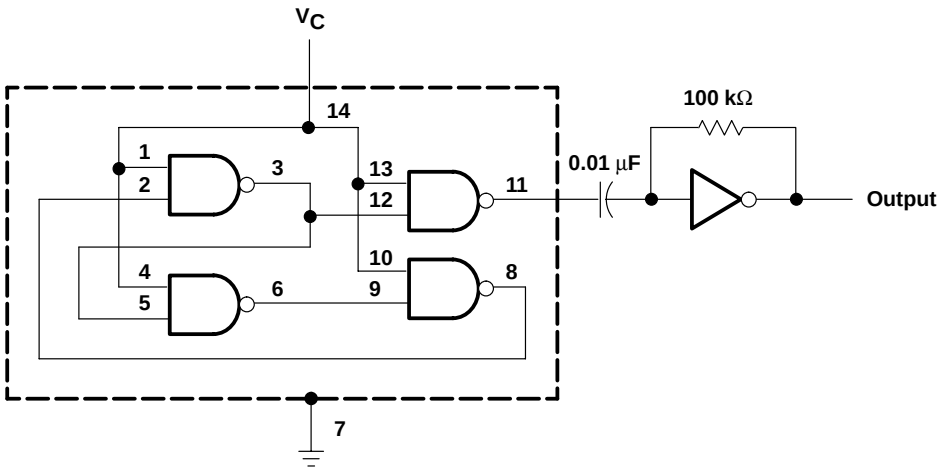


Figure 36. VCO

The inverter, which is powered by a separate voltage source, serves to restore the oscillator output voltage to 5 V, peak to peak. This function is required because the HC00 switches from rail to rail (as do all HC devices). The magnitude of the oscillator output voltage thus is dependent on V_C. The 100-kΩ resistor across the inverter provides bias such that operation is within the linear operating region of the gate. The capacitor serves as an ac-couple between the oscillator and inverter.

To prevent oscillator “bleed-through” onto the V_{CC} line, adequate decoupling of the HC device power supply is required.

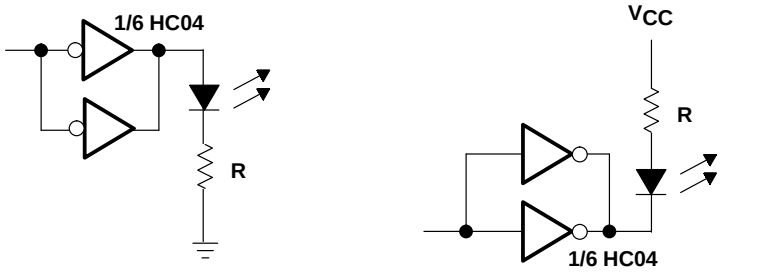
Drivers for LEDs and Relays

Introduction

Recommended operating source or sink current for HCMOS devices is 5.2 mA. Several SN74HC gates can be tied in parallel to drive LEDs and relays.

Driving LEDs

Figure 37 shows an HC04 driving a TTL221 gallium phosphide light-emitting diode. The resistor performs the function of current limiter. The luminous intensity of the LED depends on the amount of forward current.



a) V_{IL} at the Input Turns On the LED b) V_{IH} at the Input Turns On the LED

Figure 37. HC04 Driving an LED

Driving Relays

Multiple gates can be connected in parallel to increase the current-sinking or sourcing capability of SN54/74HC devices. Figure 38 shows two HC04 gates connected in parallel for a relay-driver application.

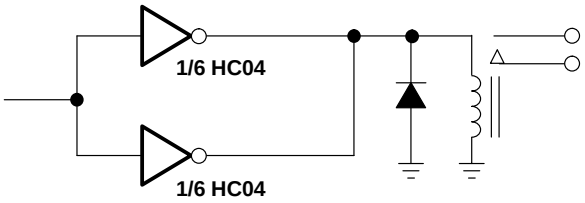


Figure 38. SN54/74HC04 Gates Connected in Parallel to Drive a Relay

SN54/74HC Interchangeability Guide

Introduction

The following has been prepared as a guide to interchanging devices from other logic families, both bipolar and CMOS, with those from the SN54/74HC family. This is not intended to be a comprehensive guide since interchangeability can depend on many factors, and only careful comparisons of data sheets can provide definitive answers. The considerations listed below are based on information accumulated in answering a large number of inquiries in this area.

First, a brief review is given on each logic technology, then a discussion is given on the various aspects involved in attempting to interchange that technology with the SN54/74HC family.

TTL: Transistor-Transistor Logic

TTL is the generic name for several bipolar families that have evolved over the last 20 years. Low-power Schottky (LS) is the most widely used bipolar logic family today. Other families, e.g., Schottky (S), advanced Schottky (AS), and advanced low-power Schottky (ALS) also are used, depending on the speed-versus-power performance required by a given system design.

4000 Series: Metal-Gate CMOS Logic

The device type numbers in this series have a variety of prefixes, although CD probably is the most widely recognized. The suffix B is used frequently, indicating an improvement over the original family; i.e., buffered outputs and typical output sink and source current capabilities of ±1 mA. This logic family became popular because it offered very low power consumption, even though it is slower than TTL, with a typical operating frequency of about 5 MHz, has a low level of ESD protection, and is susceptible to latch-up problems.

Interchangeability Considerations

Listed below are the highlights of benefits derived from replacing other logic families with SN54/74HC; also listed are important considerations that may affect the feasibility or desirability of such replacement. All comparisons are, by necessity, general in nature.

LS

Considerations:

- SN54/74HC high-level input voltages are not TTL compatible. In a mixed-family system (LS output driving HC input), it is necessary to use SN54/74HCT pullup resistors or level shifters.
- SN54/74HC has less drive capability than some LS functions.
- LS open-collector outputs have higher breakdowns than SN54/74HC open-drain equivalent functions.

HCMOS advantages:

- Lower system power consumption
- Improved noise immunity
- Wider supply-voltage range

Other TTL Families

Considerations:

- SN54/74HC high-level input voltages are not TTL compatible. In a mixed-family system (TTL output driving HC input), it is necessary to use SN54/74HCT pullup resistors or level shifters.
- SN54/74HC has less drive capability than some TTL functions.
- TTL open-collector outputs have higher breakdowns than SN54/74HC open-drain equivalent functions.
- Some of the TTL families offer greater operating speed; e.g., S, AS, and ALS.

HCMOS advantages:

- Lower system power consumption
- Improved noise immunity
- Wider supply-voltage range

4000 Series

Considerations:

- Although most applications use a 5-V supply, these older families operate in the 3-V to 15-V range.
- SN54/74HC must be operated with a supply voltage in the 2-V to 6-V range.

HCMOS advantages:

- Higher frequency of operation
- Improved ESD protection and latch-up performance
- Higher output drive capability

As a quick reference guide, Table 4 highlights the advantages and disadvantages of interchanging other logic families with high-speed CMOS.

Table 4. Highlights of Interchangeability

	TTL FAMILY (TTL, LS, S, ALS, AS)	METAL-GATE CMOS
Power	HCMOS offers lower system power consumption than any of the TTL families.	Power consumption of HCMOS is less than metal-gate CMOS.
Speed	HCMOS operating speed is comparable to LS. Some TTL families (S, AS, and ALS) offer greater operating speed.	HCMOS operating speed is much faster than metal-gate CMOS.
Input voltage	The V_{IH}min of HCMOS is not compatible with the V_{OH}min of TTL. In mixed-family systems, it is necessary to use HCT devices, pullup resistors, or level shifters.	HCMOS input voltage levels are compatible with metal-gate CMOS outputs only when the power-supply voltage for the metal-gate CMOS devices is between 2 V and 6 V.
Output voltage	The output voltages of HCMOS are TTL compatible.	HCMOS output voltage levels are compatible with metal-gate CMOS inputs only when the power-supply voltage for the metal-gate CMOS devices is between 2 V and 6 V.
Drive capability	The output current capability of HCMOS is not as large as the TTL family.	HCMOS has a higher current drive capability.
Fan-out (LS devices)	HCMOS has a smaller fan-out to LS devices than the TTL family.	HCMOS has a higher fan-out to LS devices.
Supply voltage	HCMOS has a wide operating supply-voltage range (2 V to 6 V).	Operating supply-voltage range of metal gate is larger than HCMOS (from 3 V to 15 V).
ESD and latch-up	TTL-family devices are not as vulnerable to ESD and latch-up damage.	HCMOS has an improved protection circuitry against ESD and latch-up.

In recent years, several advanced CMOS logic families have been introduced by TI. Although these advanced families do not have as wide a power-supply range as HCMOS, they have certain advantages over HCMOS families: higher speed, higher drive, lower power consumption, and a better ESD protection circuit. LVC, ALVC, and AVC are examples of these families. For details, please refer to the TI *Logic Selection Guide*.

Electrostatic Discharge (ESD)

Introduction

In recent years, the semiconductor industry has made great strides in developing faster, lower-power, and smaller devices. Over the last few years, many devices have been produced with minimum feature size of structures on a silicon chip in submicron technology. To put this in perspective, a typical human hair is about 75 μm in diameter. However, as feature sizes get smaller and smaller, ESD sensitivity (the voltage level at which the device will sustain damage) also gets lower. This means that ESD protection and ESD handling procedures will become even more important in the future to avoid ESD damage.

All semiconductor devices have an ESD voltage threshold above which they sustain damage. While circuit designers can provide some on-circuit ESD protection, this is well below the static-voltage levels found in work areas without ESD protection. Proper ESD handling and packaging procedures must be used throughout the processing, handling, and storing of unmounted ICs and ICs mounted on circuit boards.

What is ESD and How Does It Occur?

Static charge is an unbalanced electrical charge at rest. It is created by insulator surfaces rubbing together or pulling apart. One surface gains electrons while the other surface loses electrons. This results in an unbalanced electrical condition known as static charge.

When a static charge moves from one surface to another, it becomes ESD. ESD is a miniature lightning bolt of static charge that moves between two surfaces that have different potentials. It can occur only when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When static charge moves, it becomes a current that damages or destroys oxides, metallizations, and junctions. ESD can occur in any one of four different ways: a charged body can touch an IC, a charged IC can touch a grounded surface, a charged machine can touch an IC, or an electrostatic field can induce a voltage sufficient to break down the dielectric.

Latent Defects

Devices with latent ESD defects are called “walking wounded” because they have been degraded but not destroyed by ESD. This occurs when an ESD pulse is not sufficiently strong to destroy a device but, nevertheless, causes damage. Often, the device suffers junction degradation through increased leakage or a decreased reverse breakdown, but the device still functions and is still within data-sheet limits. A device may be subjected to numerous weak ESD pulses, producing cumulative degradation until the device fails. There is no known practical screen for walking-wounded devices. To avoid this type of damage, devices must have continuous ESD protection, as outlined later.

What Voltage Levels of ESD Are Possible?

It has been shown that human beings can be charged up to 38,000 V just by walking across a rug on a low-humidity day. For an ESD pulse to be seen, felt, or heard, it must be in the range of 3000 V to 4000 V. Many devices can be damaged well below this threshold.

How to Avoid ESD Damage to ICs

Because ESD can occur only when different potentials are involved, the best way to avoid ESD damage is to keep the ICs at the same potential as their surroundings. The logical reference potential is ESD ground. So, the first and most important rule in avoiding ESD damage is to keep ICs and everything that comes in close proximity to them maintained at ESD-ground potential. Four supplementary rules support this first rule:

- Any person handling the ICs should be grounded either with a wrist strap or ESD-protective footwear used with a conductive or static-dissipative floor or floor mat.
- The work surface where devices are placed for handling, processing, testing, etc., must be made of static-dissipative material and be grounded to ESD ground (see Figure 39).
- All insulator materials must either be removed from the work area or they must be neutralized with an ionizer. Static-generating clothing can be covered up with an ESD-protective smock.
- When ICs are being stored, transferred between operations or workstations, or shipped, they must be maintained in a Faraday-shield container whose inside surface (touching the ICs) is static dissipative.

Humidity

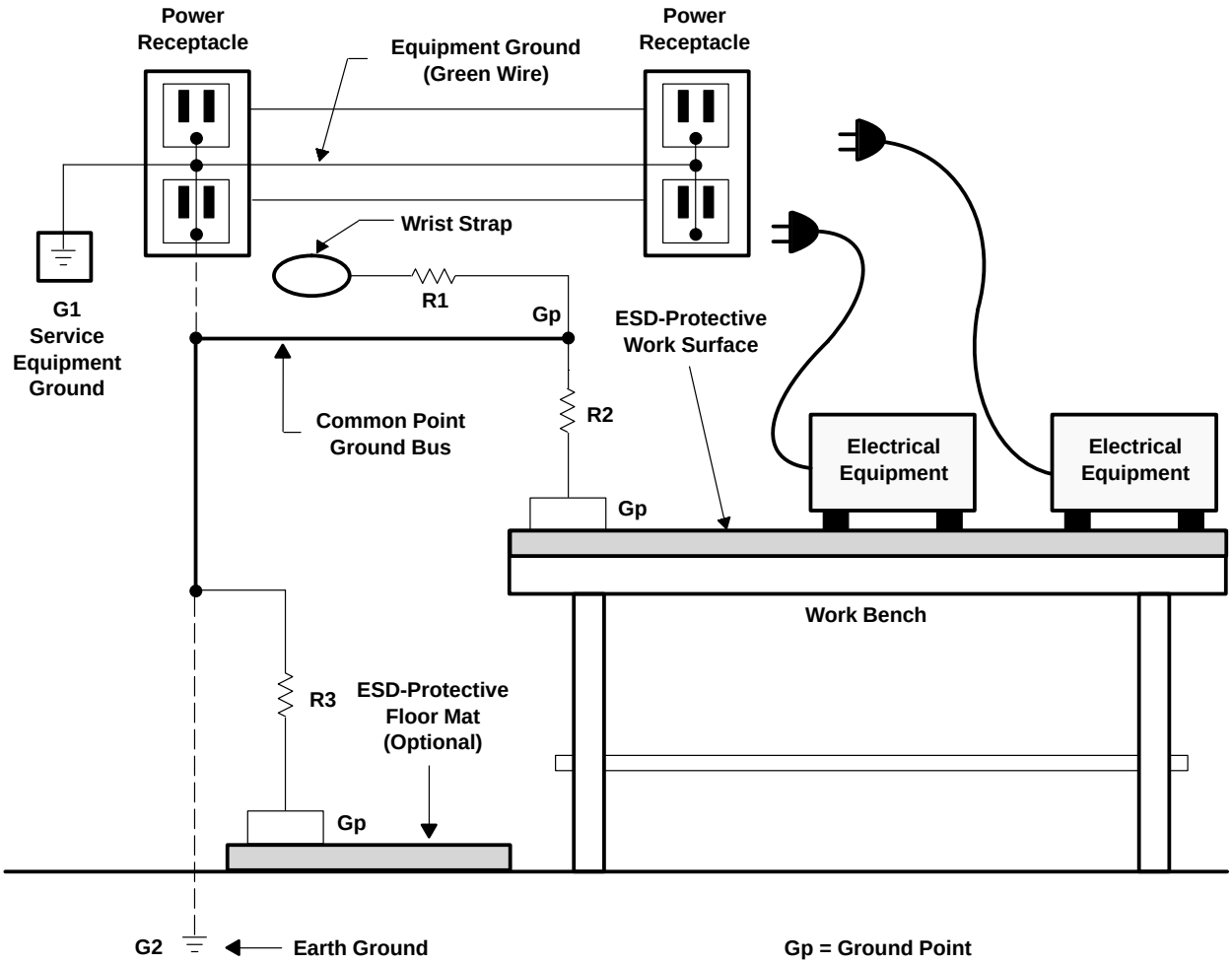
Where insulators are present, humidity is a very important factor in the generation of static electricity. Humidity affects the surface resistivity of insulator materials. As humidity increases, the surface resistivity decreases. This means that insulator materials rubbed together or pulled apart in a humid environment generate lower static charges than the same materials rubbed together or pulled apart in a dry environment. Where it is possible to control humidity, it is recommended that relative humidity be maintained between 40 percent and 60 percent. Higher humidity becomes very uncomfortable for humans, and lower humidity increases the risk of static generation from insulators. Humidity is a supplementary control and is not sufficient by itself to reduce static voltages to safe levels.

Training

All personnel who come in close proximity to ESD-sensitive ICs must receive ESD training initially and then again each year as a minimum. No ESD program can be successful unless the people who handle the ICs understand the need for ESD controls.

ESD Specification

Each area handling ESD-sensitive devices is operated in accordance with the established ESD handling procedure. The latest version of this controlled document is maintained in each area and is accessible to all area personnel.



NOTES:
1. G1 (equipment ground) or G2 (earth ground) is acceptable for ESD ground. Where both grounds are used, they are connected (bonded) together.
2. R1 is mandatory for all wrist straps.
3. R2 (for static-dissipative work surfaces) and R3 (for ESD-protective floor mats) are optional. ESD-protective flooring is connected directly to the ESD ground without R3.
4. This ESD-protected workstation complies with JEDEC Standard No. 42 and EIA-625.

Figure 39. ESD-Protected Workstation (Side View)

ESD Coordinator

One person is identified who has overall responsibility for the ESD program. This person is responsible for writing the ESD handling procedure and keeping it updated, ESD training, and material evaluation.

Audits

Periodic audits ranging from daily to yearly are held to ensure that all ESD handling procedures are being followed and that all ESD materials (wrist straps, heel straps, ionizers, table mats, floor mats, etc.) are functioning properly.

TI ESD Handling Procedure

The TI worldwide ESD handling procedure is available to customers upon request.

Moisture Sensitivity of Plastic Surface-Mount Packages

Some plastic surface-mount packages are classified as moisture sensitive because the moisture that has been absorbed inside the package can expand rapidly during exposure to the fast-rise-time, high-temperature stress of reflow soldering and mechanically damage the package (often referred to as “popcorn”). Surface-mount packages are subjected to much higher solder reflow temperatures than their through-hole counterparts. The bodies of the through-hole parts are shielded from the hot-wave solder by the PC board, while surface-mount parts are subjected to the full solder reflow temperature.

All plastic packages absorb some moisture at room ambient conditions. The amount of moisture absorbed is based on a number of factors, including room temperature and humidity. However, there is no threshold level of moisture absorption or gain that applies to all plastic surface-mount packages that makes them moisture sensitive. Conversely, all plastic surface-mount packages that essentially are moisture-free during reflow soldering will be free of moisture-induced stress failures.

It is important, therefore, to know which packages are moisture sensitive so they can receive special care in handling to minimize moisture absorption and subsequent moisture-induced stress damage during the reflow soldering operation.

At TI, plastic surface-mount packages are tested for moisture sensitivity using JEDEC test method A112, Moisture-Induced Stress Sensitivity for Plastic Surface-Mount Devices. Packages that are found to be moisture sensitive are baked (to drive out the moisture) and then placed in a protective dry-pack bag that contains a humidity indicator card and sufficient desiccant to maintain a very low humidity level in the bag. A caution label (as defined in JEDEC publication 113) is attached to the bag and indicates the minimum floor life of the packages once they are removed from the protective dry environment of the bag. There are seven possible moisture sensitivity levels (two in Level 5) as shown in the table below. JEDEC publication 113 defines the labels required for each level.

LEVEL	DRY-PACK BAG/LABEL REQUIRED?	FLOOR LIFE @ 30°C, 60% RH
1	No	No limit
2	Yes	1 year
3	Yes	168 hours
4	Yes	72 hours
5	Yes	24 or 48 hours (noted on label)
6	Yes	6 hours after mandatory bake

Plastic surface-mount packages that are not moisture sensitive per JEDEC test method A112 do not need to be dry packed or handled in a special way to minimize moisture absorption prior to reflow soldering, provided that the package body temperature does not exceed 220°C during reflow soldering.

Floor life is defined as the time after the devices have been removed from the protective dry-pack bags until the devices are subjected to reflow soldering. If this floor life is exceeded, there are instructions on the dry-pack bag label indicating how long the devices must be baked, and at what temperature, to restore them to a safe condition for reflow soldering.

Dry packing is a method of controlling the moisture absorption during shipping and storage. All product that is classified as moisture sensitive with a rating of 2, or higher, is dry packed and labeled as moisture sensitive, with the bag label outlining the necessary precautions for handling the product. As long as the devices are rated as moisture sensitive, dry packing is used, regardless of whether the components are shipped in tubes (magazines), tape and reel, or trays. Components rated as nonmoisture sensitive (Level 1) need not be baked and dry packed.

The dry-packing process starts at the manufacturer’s final packing stage. The components are initially baked and then placed inside a moisture-vapor barrier bag along with desiccant to absorb moisture and keep the humidity inside the bag at a safe level (<20% RH).

The customer should check the humidity indicator immediately after opening the bag to determine whether the moisture level has been exceeded. If the 20% dot on the humidity indicator card is pink and the 30% dot is not blue, the components have been exposed to an excessive moisture level and should be rebaked before being subjected to the surface-mount process. If baking is required, devices may be baked for:

- 192 hours at 40°C + 5°C/–0°C and <5% RH for all component containers (tray, magazines, or tape and reel); or
- 24 hours at 125°C ±5°C for device containers rated at 125°C or above

Moisture-sensitive components can be resealed in their original bag with the original desiccant if:

- Humidity indicator card shows 20% RH
- Components have not been out of the bag for more than 2 hours, and
- Components have not been exposed to conditions greater than 30°C/60% RH

If the 2 hours of exposure is exceeded, the floor life should be adjusted accordingly. Reduce the floor-life level by 1 hour for each hour over the 2-hour limit the material is out of the bag. For example, if the rating is Level 4 and the material has been out for 4 hours, the floor life shown on the label is reduced from 72 hours to 70 hours (suggestion: close bag within 10 minutes after any opening).

Total time out of the bag is cumulative. Each time the bag is opened and resealed, the corresponding time out of the bag should be deducted from the remaining floor life. This process may be repeated until the floor-life hours are used up, in which case rebaking of the remaining components is required. Rebaking would return the residual components to the original Level-4 status, with the corresponding floor life of 72 hours.

The moisture indicator cards should be used to assist in monitoring the moisture level and maintaining control of the humidity below the 20%-RH level. If there is any doubt as to the moisture condition of the parts, baking is recommended to restore the components to a safe, usable condition, ready for board assembly.

Conclusion

Within the constraints given above, the SN54/74HC family can be regarded as a pin-for-pin equivalent to the other logic families. The SN54/74HC family is ideally suited for system upgrading, system shrinking, or especially, new system design.