APPLICATION NOTE

Low voltage FM stereo radio with TEA5767/68

AN10133

Philips Semiconductors

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Abstract

This document describes an application in which the FM stereo radio **TEA5767/68** is being used. This new generation single-chip stereo radio is alignment free. Because of its low power consumption, small size and small FM application, this tuner will lead to a breakthrough in the market of portable consumer products, as mobile phone, CD and MP3 players.

The radio can tune into the European, Japan and US FM bands.

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Summary

The TEA5767/68 is a single chip stereo FM receiver. This new generation low voltage FM radio has a fully integrated IF-selectivity and demodulation. The IC does not require any alignment, which makes the use of bulky and expensive external components unnecessary.

The digital tuning is based on the conventional PLL concept. Via software, the radio can be tuned into the European, Japan or US FM band.

The power consumption of the tuner is low. The current is about 13mA and the supply voltage can be varied between 2.5 and 5V.

The radio can find its application in many areas especially portable applications as mobile phones, CD and MP3 players.

This application note describes this FM radio in a small size and low voltage application. To demonstrate the operation of the tuners a demoboard is developed, which can be extended with a software controllable amplifier and a RDS chip. The whole application can be controlled from a PC by means of demo software.

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1 INTRODUCTION

The consumer demand of more integrated and low power consumption IC's has increased tremendously in the last decade. The IC's must be smaller, cheaper and consume less power. Especially for portable equipment like mobile phone, CD, MP3 and cassette players, these requirements are very important. In order to integrate a radio function in this kind of equipment it's also important that the total application is small sized and the overall power is low. The **TEA5767/68** is a single chip digitally tuned FM stereo radio. Its application is small, has a very low current consumption and is completely adjustment free. This makes the PCB design easy and save design-in time. The tuner contains all the blocks necessary to build a complete digitally tuned radio function.

The FM tuners consist of three IC's in 32 pins or 40 pins package. The IC's can be controlled via a 3-Wire, I2C or both bus interfaces.
A small application PCB demo board has been designed on which either of the three IC's can be mounted. These demo boards can be placed on a motherboard, which can be extended with an audio amplifier and a **R**adio **D**ata **S**ystem (**RDS/RBDS)** IC.

The three tuners are:

- TEA5767HN FM stereo radio, 40 leads with I^2C and 3-Wire bus interface, Body 6*6*0.85 mm, SOT1618
- TEA5767HL FM stereo radio, 32 leads with 3-Wire bus interface, Body: 7*7*1.4 mm, SOT358.
- TEA5768HL FM stereo radio, 32 leads with I^2C bus interface, Body: 7*7*1.4 mm, SOT358.

In this application note only one IC, the TEA5767HN and one demo board will be described. However, this description can also be applied for the other boards.

2 SYSTEM GLOBAL VIEW

2.1 The TEA5767

A block diagram of the TEA5767HN is given in Figure 1. The block diagram consists of a number of blocks that will be described according to the signal path from the antenna to the audio output.

The RF antenna signal is injected into a balanced low noise amplifier (LNA) via a RF matching circuit. In order not to overload the LNA and the mixer the LNA output signal is fed to an automatic gain control circuit (AGC). In a quadrature mixer the RF signal is converted down to an IF signal of 225KHz by multiplying it with a local oscillator signal (LO). The chosen mixer architecture provides inherent image rejection.

The VCO generates a signal with double the frequency necessary for the I/Q mixer structure. In the N1 divider block, the required LO signal is created. The frequency of the VCO is controlled with a PLL synthesiser system. The I/Q signals out the mixer are fed to an integrated IF filter (RESAMP block). The IF frequency of this filter is controlled by the IF Centre Frequency adjust block.
The IF signal is then passed to the limiter block, which removes the amplitude variation from the signal. The limiter is connected to the level ADC and the IF counter blocks. These two blocks provide the proper information about the amplitude and frequency of the RF input signal, which will be used by the PLL as stop criterion.
The IC has a quadrature demodulator with an integrated resonator. The demodulator is fully integrated which makes IF alignments or an external resonator unnecessary.

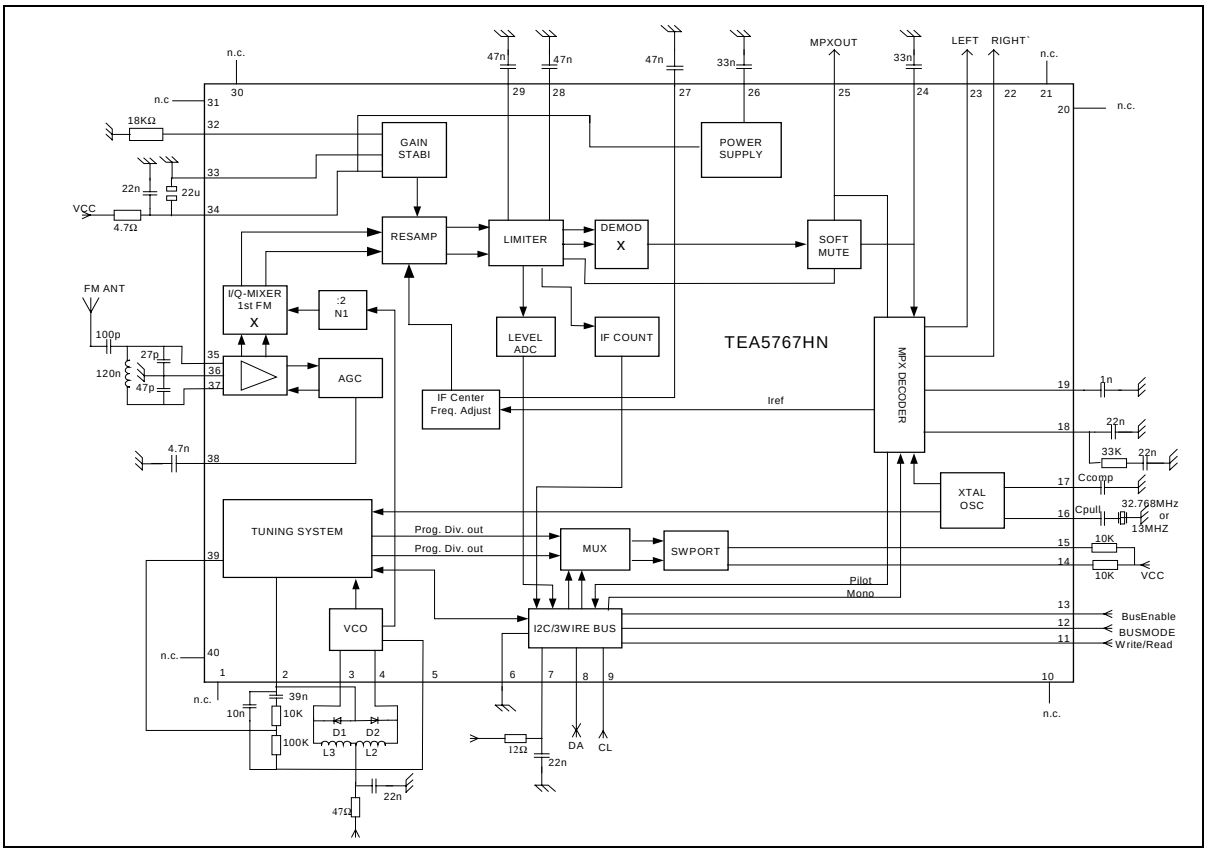


Figure 1 Block application diagram of the TEA5767HN

The **stereo decoder (MPX decoder)** in its turn is adjustment free and can be put in mono mode from the bus interface.
The stereo noise cancelling (SNC) function gradually turns the stereo decoder from 'full stereo' to mono under weak signal conditions. This function is very useful for portable equipment since it improves the audio perception quality under weak signal conditions.

The softmute function suppresses the interstation noise and prevents excessive noise from being heard when the signal level drops to a low level.

The tuning system is based on a conventional PLL technique. This is a simple method in which the phase and the frequency of the VCO are continuously corrected, with respect to a reference frequency, until frequency acquisition takes place.

Communication between the tuning system and an external controller is possible via a 3-Wire or I^2C bus interface.

2.2 FM STEREO application

The application is identical for the three IC's as mentioned in chapter 1. This application comprises two major circuits: RF input circuit and a FM oscillator circuit.

The communication with a μ-computer can be performed via an I^2C or a 3-Wire serial interface bus, selectable with BUSMODE pin, for the TEA5767HN. TEA5768HL operates in I^2C bus mode and TEA5757HL in 3-Wire bus mode.

The receivers can work with 32.768KHz or 13MHz clock crystal, which can be programmed by the bus interface. The PLL can also be clocked with 6.5MHz clock signal.

Three audio outputs are available: audio left, audio right and MPX (multiplex).
A basic application diagram of the FM receiver is shown in Figure 2.

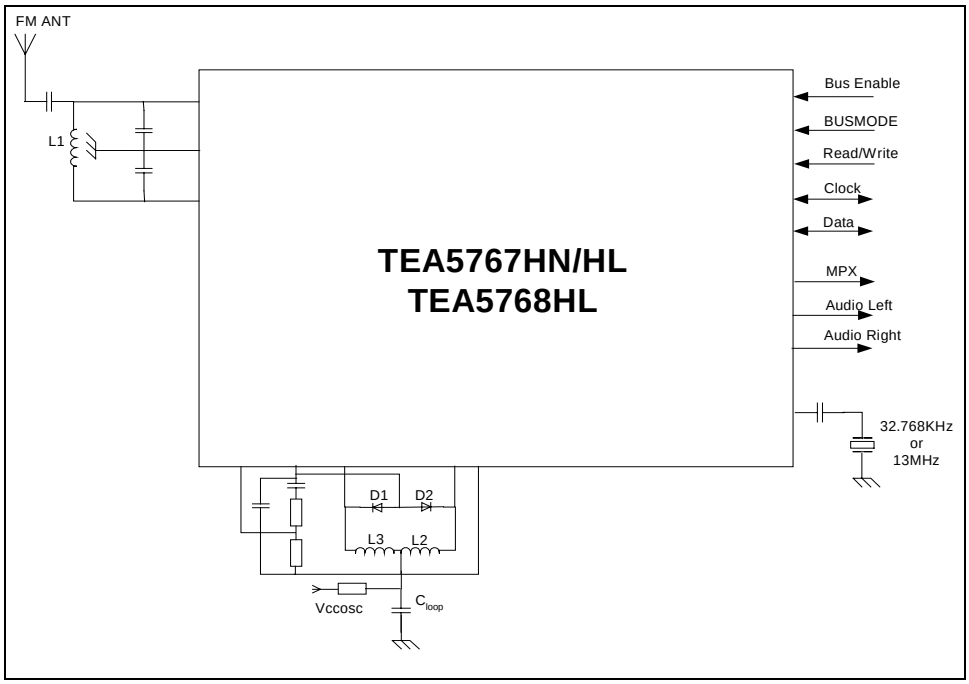


Figure 2 Basic application diagram of TEA5767/68 stereo radio

2.3 TEA5767HN package

The TEA5767HN FM stereo radio is a 40 pins HVQFN (SOT1618) package IC which can be operate with I^2C or 3-Wire bus interface. The fully integrated IF selectivity and demodulation make it possible to design a very small application board with a minimum of very small and low cost components. The outline of the TEA5767HN package is 6*6*0.85 mm.

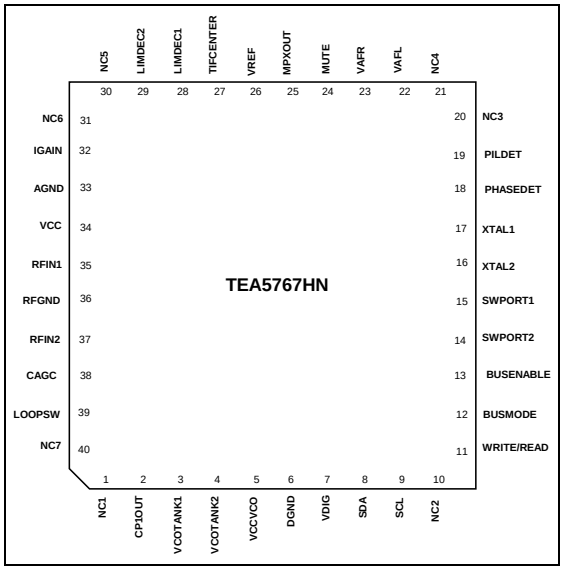


Figure 3 Pinning of the TEA5767HN (HVQFN40)

Figure 3 shows the pinning of the TEA5767HN and Table 1 gives a description of each pin of the IC.

SYMBOL	PIN	DESCRIPTION	Voltage min.	SYMBOL	PIN	DESCRIPTION	Voltage min.
NC1	1	Not connected		NC4	21	Not connected	
CPOUT	2	Charge pump output of the synthesiser PLL	1.64V	VAFL	22	Audio left output	
VCOTANK1	3	VCO tuned circuit output 1	2.5V	VAFR	23	Audio right output	
VCOTANK2	4	VCO tuned circuit output 2	2.5V	TMUTE	24	Time constant for the softmute	1.5V
VCCVCO	5	VCO supply voltage	2.5V	MPXOUT	25	FM demodulator MPX out	
DGND	6	Digital ground	0V	VREF	26	Reference voltage	1.45V
VDIG	7	Digital supply voltage	2.5V	TIFCENTER	27	Time constant for IF centre adjust	1.34V
DATA	8	Bus data line input/output		LIMDEC1	28	Decoupling IF limiter 1	1.86V
CLOCK	9	Bus clock line input		LIMDEC2	29	Decoupling IF limiter 2	1.86V
NC2	10	Not connected		NC5	30	Not connected	
WRITE/READ	11	Write/read control for the 3-Wire bus		NC6	31	Not connected	
BUSMODE	12	Bus mode select input		IGAIN	32	Gain control current for IF filter	0.48V
BUSENABLE	13	Bus enable input		AGND	33	Analog ground	0V
SWPORT1	14	Software programmable port 1		VCC	34	Analog supply voltage	2.5V
SWPORT2	15	Software programmable port 2		RFIN1	35	RF input 1	0.93V
XTAL1	16	Crystal oscillator input 1	1.64V	RFGND	36	RF ground	0V
XTAL2	17	Crystal oscillator input 2	1.64V	RFIN2	37	RF input 2	0.93V
PHASEDET	18	Phase detector loop filter	1.0V	CAGC	38	Time constant RF AGC	
PILDET	19	Pilot detector lowpass filter	0.7V	LOOPSW	39	Switch output of synthesiser PLL filter	
NC3	20	Not connected		NC7	40	Not connected	

Table 1 pinning description of the TEA5767HN

3 THE TEA5767HN

The TEA5767HN consists of three major blocks: the signal channel, the tuning system and the bus interface. In this chapter the signal channel will be described briefly. The tuning system and the interface will be explained in chapter 4 receptively 5.

In Figure 4, a block diagram of the signal path is given.

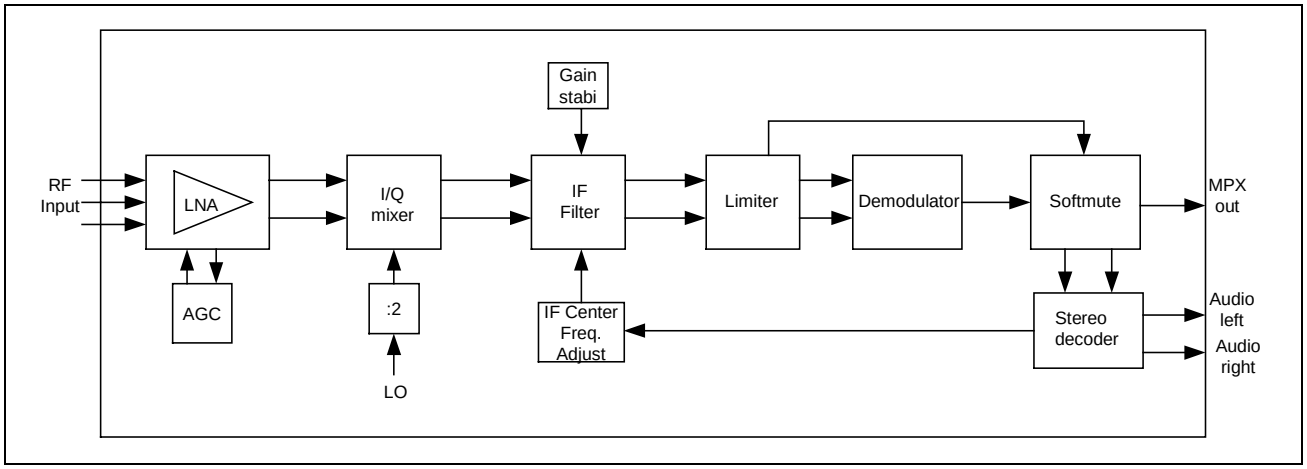


Figure 4: Block diagram of the signal path of the tuner

3.1 Low Noise Amplifier

The TEA5767HN has an integrated low noise amplifier (LNA). This is a balanced amplifier, which is less sensible for common mode noise.

The input impedance of the LNA is (100Ω||4pF) each pin (referenced to ground).

To handle high level input signals, the gain of the LNA is controlled by means of an automatic gain controller (AGC). The AGC will be started when the antenna input reaches a level of about 4mV with a given application of 40Ω antenna impedance. The AGC has a range of 40dB.

3.2 Mixer

The TEA5767HN has a complex mixer. This mixer receives two RF signals directly from the LNA and delivers two signals with an intermediate frequency of 225KHz. The mixer output signals comprise an in-phase component (0^0) and a quadrature component (90^o).

A block diagram of the mixer is given in Figure 5.

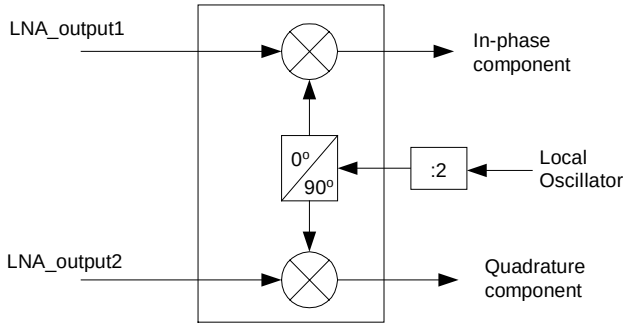


Figure 5: block diagram of the quadrature mixer

Theoretically, complex mixers can create perfect image cancellation and do not need an image rejection filter. However, because of imperfection in the channel end or LO divider signals, the tuner will have a limited image rejection problem.

3.3 IF selectivity

The selectivity is provided by a band pass filter with a low intermediate frequency (IF). This IF filter is fully integrated, which results in an alignment-free selectivity. The centre frequency of this filter is 225KHz and has a –3dB bandwidth of 90KHz.
At 200KHz from the centre frequency, the IF filter selectivity is about 40dB.

The centre frequency of the IF filter is internally adjusted in order to remove the influence of process spread.

3.4 Limiter

The limiter is DC coupled with feedback capacitors on pin 28 and 29. These capacitors build a low pass filter.

3.5 Demodulator

The demodulator is also fully integrated. The advantage of this is that no alignment will be necessary.
The demodulator has a conversion factor of 75mV at 22.5kHz.

3.6 The MPX decoder

3.6.1 The PLL

The stereo decoder PLL runs at 228kHz (12*19KHz). When using a crystal of 13MHz, the VCO is internally preset to 227.5KHz. The frequency sensitive phase detector can only accelerate the VCO. After the PLL is locked on the proper frequency (228KHz), it will become inactive.

When the crystal clock frequency is changed the principle stays the same. The PLL in a locked situation is still running at 228KHz. The preset frequency, however, is now 229.4KHz. In this situation, the phase detector can only slow down the VCO until the PLL is locked on 228kHz.

A divider delivers a quadrature 19KHz signal, which will be multiplied with the 19KHz spectral component of the MPX signal. When there is a phase difference between the two signals, a dc current is generated that will adjust the VCO until synchronisation has taken place.
Care should be taken with the capacitors used in the loop filter (pin 18 of TEA5767HN). Any leakage current due to these capacitors will affect the PLL VCO free running frequency and will reduce the capture range and channel separation. Therefore, capacitors with a stable temperature coefficient are recommended.

3.6.2 The pilot detector

Via a divider circuit, the PLL stereo decoder will deliver the 19kHz, 0^o signal to the pilot detector. This signal will be multiplied with the pilot present in the MPX signal. This will give a DC signal that is proportional with the pilot amplitude.
The pilot filter will remove the audio information and the 38kHz components. Figure 6 gives a block diagram of the pilot detector.

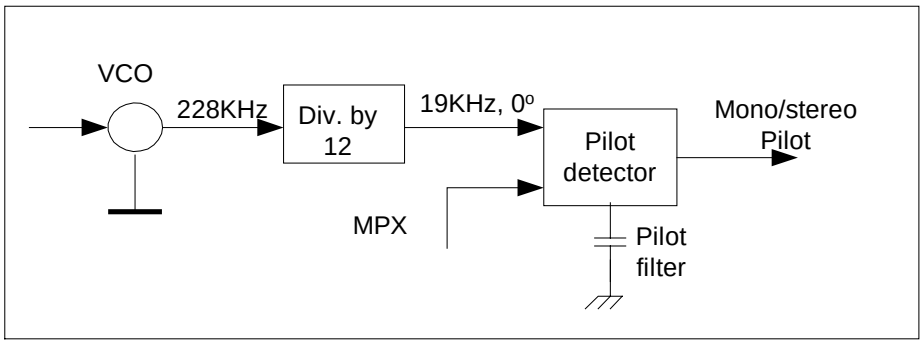


Figure 6 Pilot detector of the MPX decoder

Bit 7 of byte 3 gives an indication of stereo reception. When this bit is high the reception is stereo otherwise mono. Leakage current due to the pilot filter will decrease the pilot sensitivity. This can lead to erroneous indication of the stereo reception

3.6.3 The SNC

When the Stereo Noise Cancelling -also named SDS (Signal dependant stereo)- is on, it will switch the stereo decoder from stereo to mono in case a weak signal is received. This will limit the output noise of the decoder. Also by the absence of the pilot or when the stereo control is switched to “force mono”, switching SNC on or off will not affect the audio reception so that only mono information will be passed to the audio output
The SDS can be switched via the bus with bit 1 of data byte 4.

Figure 7 gives a typical measurement of the audio signal and noise with SNC on and SNC off.

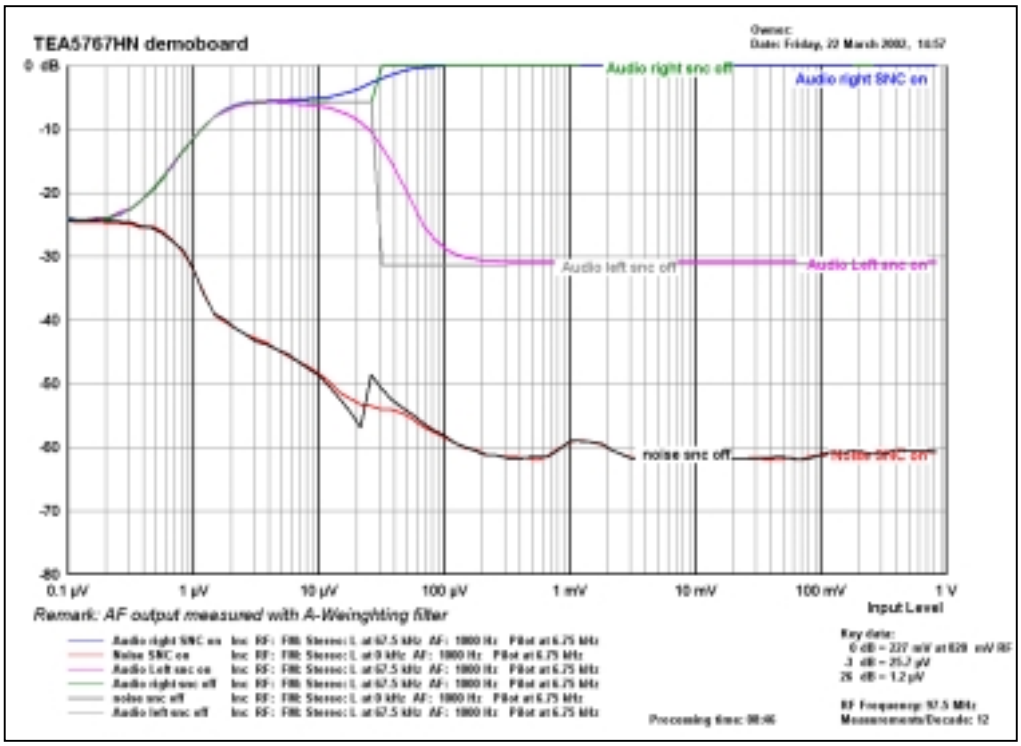


Figure 7 Effect of the SNC on the signal and noise

3.6.4 The matrix decoder

The matrix decoder calculates the audio left and right signals and delivers them to the outside of the IC via pin 22 and 23.

3.6.5 HCC

High Cut Control is an option, which gives the possibility to cut high frequencies from the audio signal when a weak signal is received.
The HCC can be switched via the bus with bit 2 of data byte 4.

Figure 8 illustrates the influence of the HCC op the audio signal and noise.

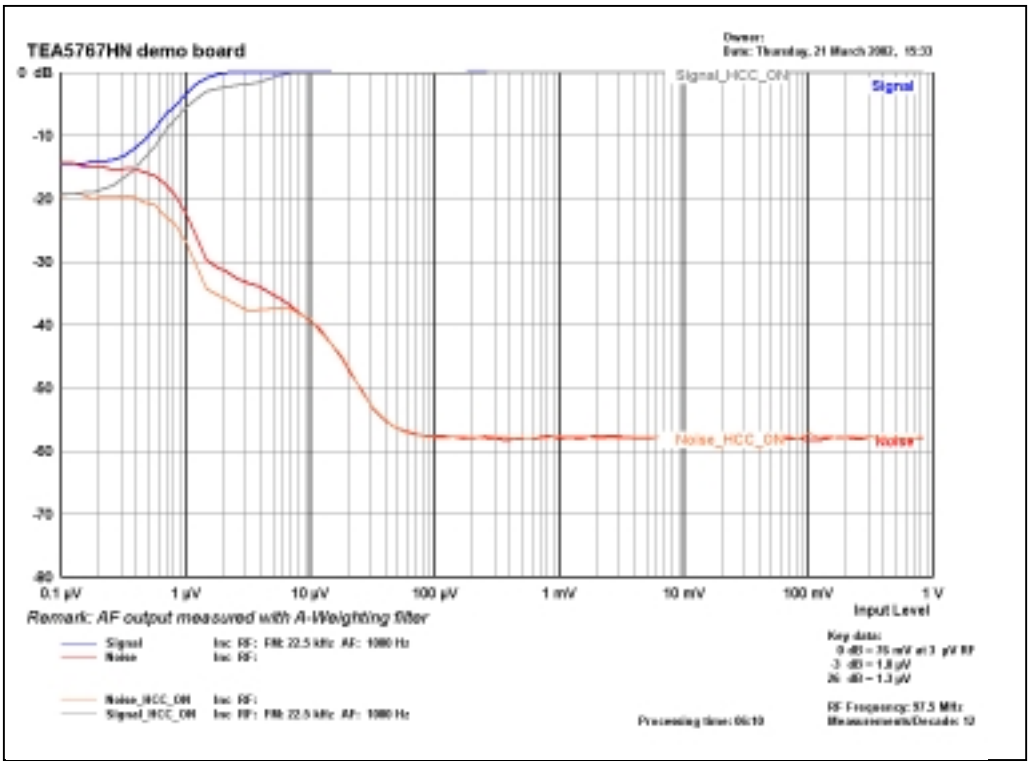


Figure 8 influence of the HCC on audio signal and noise

3.7 The softmute

The RF input signal can come under weak level input so that the total noise energy in the AF spectrum can be larger than the AF signal. This causes an unpleasant sound. When activated, the softmute will limit the amount of noise energy in the AF spectrum. The inter-station noise is then attenuated which will result in a better perception of the audio signal.
The softmute is controllable via the bus interface. By setting bit 3 of data byte 4, the softmute is switched on. Otherwise it is off.

Figure 9 illustrates the working of the softmute.

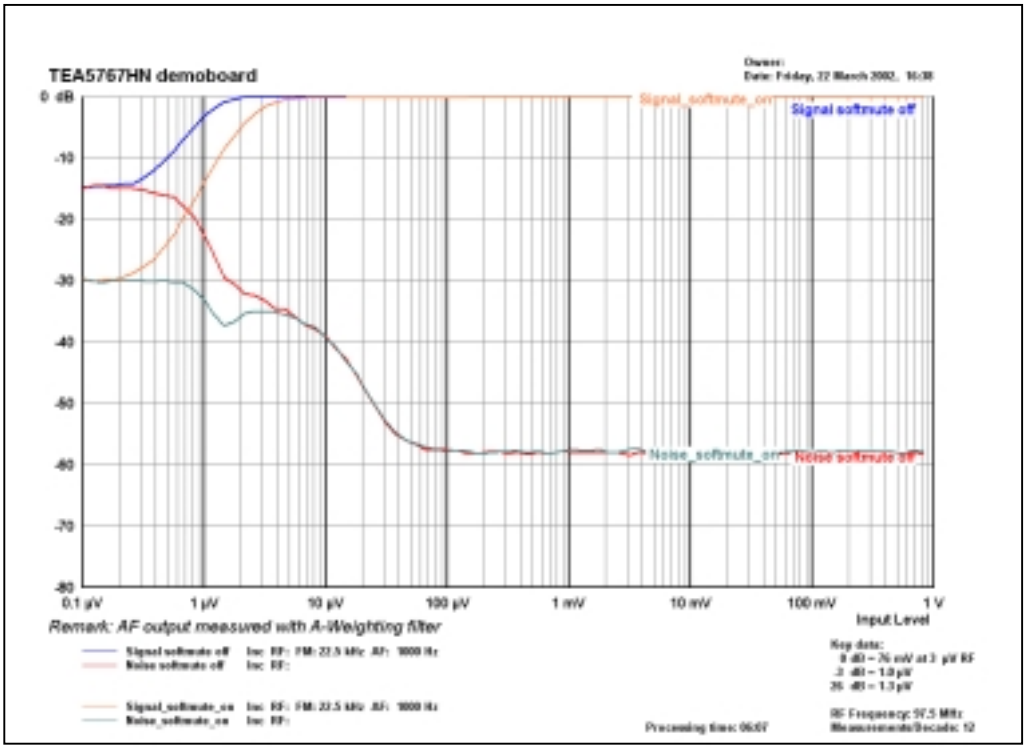


Figure 9 effect of the softmute on the signal and noise at the audio output

4 THE TUNING SYSTEM

The TEA5767HN tuning system is based on a conventional PLL technique. The tuning system is controlled by means of state machine.

In this chapter the tuning system, level ADC and IF counter will be described.

4.1 The PLL tuning system

The tuning system is based on the conventional PLL technique. This is a very simple concept in which the programmable divider is stepwise increased or decreased until a signal is found.

In a phase detector (PD) the output signal of the programmable divider is compared to a reference frequency. The PD steers a chargepump, which via a loop filter will deliver the necessary tune current to the VCO. The PLL uses two loop filters with different time constants. At the first stadium, the loop must be fast for quick response but later the loop should have a narrow bandwidth to limit noise contribution in order to achieve a good signal to noise ratio.

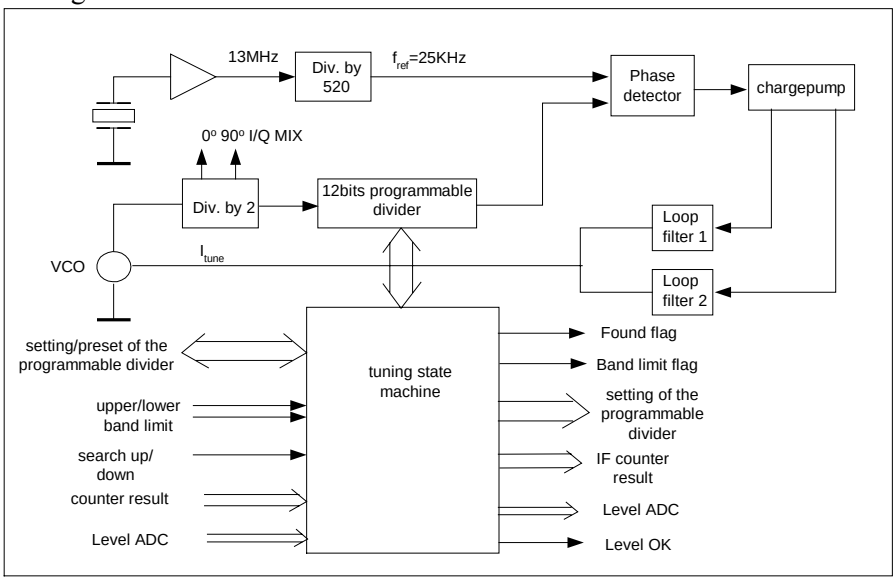


Figure 10: tuning system with a 13MHz crystal clock

The PLL synthesiser can operate with either 32.768KHz or 13MHz crystal clocks. The choice for 13MHz is due to the fact that this frequency is utilised in mobile phones so that an extra crystal is not necessary in that kind of application. The 32768Hz clock signal makes it possible to use the cheap watch crystal.
Further it is possible for the synthesiser to be clocked externally with 13MHz, 6.5MHz or 32768Hz clock signal (see pragraph 6.3.3, page 38).

In Figure 10 and Figure 11, a block diagram of the tuning system is given when using a 13MHz crystal respectively 32768Hz.

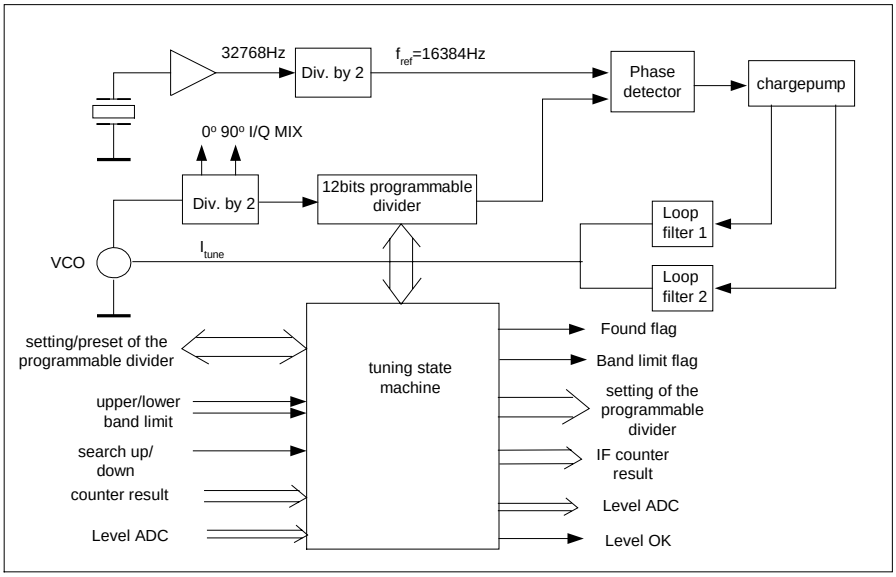


Figure 11: PLL synthesiser with 32768Hz crystal clock

In contrast to most tuner systems that use an IF of 10.7MHz, the TEA5767/68 uses a low IF of 225KHz. With this low IF, integration of the IF filter becomes feasible. This aims to reduce the overall system costs and power. Further the tuner can work in two modes: high side injection or low side injection. The choice of one of these modes determines whether the local oscillator is placed above or below the wanted frequency (see Figure 12 and Figure 13), swapping the image with respect to the reception frequency. This feature is added due to the practical achievable image suppression that can be obtained (see paragraph 4.5).
As the figures illustrate, the image frequency is situated at 450KHz (2*IF) distance below or above the wanted frequency. In software, the HILO bit can used to put the tuner in high side injection mode (HILO=1) or low side injection (HILO=0). The HILO bit is bit 4 of data byte 3.

4.2 PLL word calculation

To tune the radio to a wanted frequency, the corresponding PLL word must first be calculated. This is a 14 bits word, which will be sent to the programmable divider.
To do this a distinction will be made between high and low side injection.

4.2.1 High side injection tuning

In high side injection mode the PLL word is calculated with the following formula:

$$N_{DEC} \equiv \frac{\left(4*(F_{RF} + F_{if})\right)}{F_{REFS}} \quad \text{with:}$$

N_{DEC} = Decimal value of PLL word
F_{RF} = the wanted tuning frequency [Hz}
F_{if} = the Intermediate Frequency [Hz]
F_{REFS} = the reference frequency [Hz}

In the PC control software this is implemented in the following way:

$$PLL \equiv ROUND\left[\frac{4*(TunedFrequency*1000+F_{if})}{\frac{REF[XTAL]}{1000}}\right]$$

$PLL = N_{DEC}$ = Decimal value of PLL word
TunedFrequency is the wanted tuning frequency in **MHz**,
F_{if} is the Intermediate Frequency of 225 kHz,
REF[XTAL] is the reference frequency in **kHz**, which depends on the selection of the oscillator frequency as shown in the table below:

XTAL	PLL REF	Reference frequency	Crystal frequency
0	0	50000 Hz	13 MHz
0	1	50000 Hz	6.5 MHz
1	0	32768 Hz	32.768 kHz
1	1	32768 Hz	32.768 kHz

Table 2: VCO reference frequency versus the crystal frequency

Now that The PLL word has been calculated in decimal, it must be converted to Hex decimal before sending in to the tuning system.

If the receiver has to be tuned to a FM frequency of 100MHz, the PLL word will be calculated as follow:

$$PLL_{DEC} \equiv ROUND\left[\frac{4*(100*1000+225)}{\frac{50000}{1000}}\right] = 8018$$

$$PLL_{HEX} \equiv 1F52$$

Figure 12 gives an example of frequency tuning with high side injection.

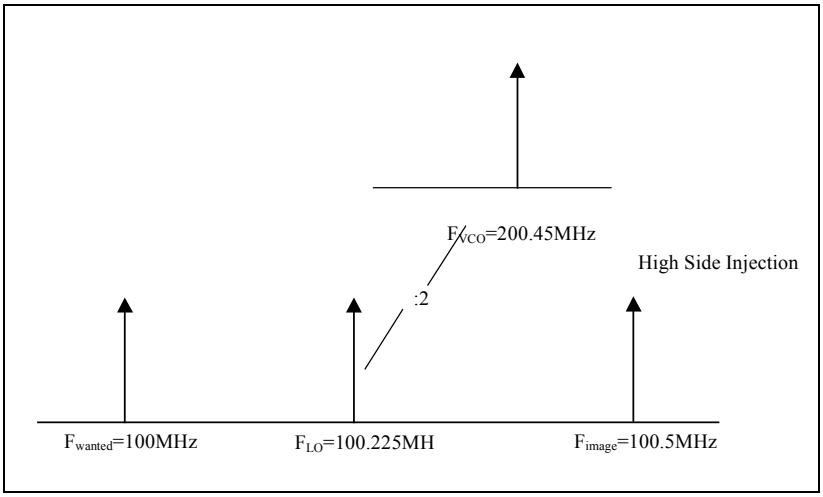


Figure 12: Example of PLL frequency calculation: high side injection

4.2.2 Low side injection tuning

To calculate the PLL word in low side injection mode the following formula is used:

$$N_{DEC} \equiv \frac{\left(4*(F_{RF} - F_{if})\right)}{F_{REFS}}$$

The parametrs stay the same as for high side injection.

To tune the tuner for example to 100MHz, the PLL word can be calculated as follow:

$$PLL_{DEC} \equiv ROUND\left[\frac{4*(100*1000-225)}{\frac{50000}{1000}}\right] = 7982$$

$$PLL_{HEX} \equiv 1F2E$$

Figure 13 illustrates a frequency tuning when low side injection mode is applied.

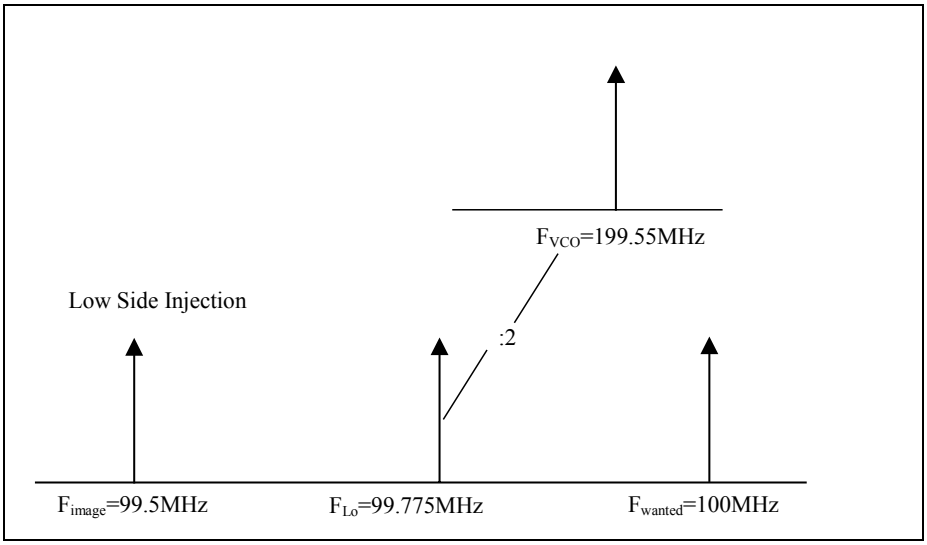


Figure 13: Example of PLL frequency calculation: low side injection

4.3 IF counter

To measure the intermediate frequency (225KHz) of the receiver, the tuning system uses a 7 bit IF counter (see Figure 14). During a time window the IF counter will count the limited IF signal. The counter counts during a measurement time which is15.75ms for 13MHz crystal and 15.625ms for a 32768 clock, with a resolution of 4062.5Hz respectively 4096Hz.
If the Level_OK signal = “1”, the state machine of the tuning system will start the IF counter. At the end of the measurement time, the counter produces a value that is an indication of the intermediate frequency. The counter result will be delivered to the tuning system for evaluation.

Table 3 gives possible correct counter results.

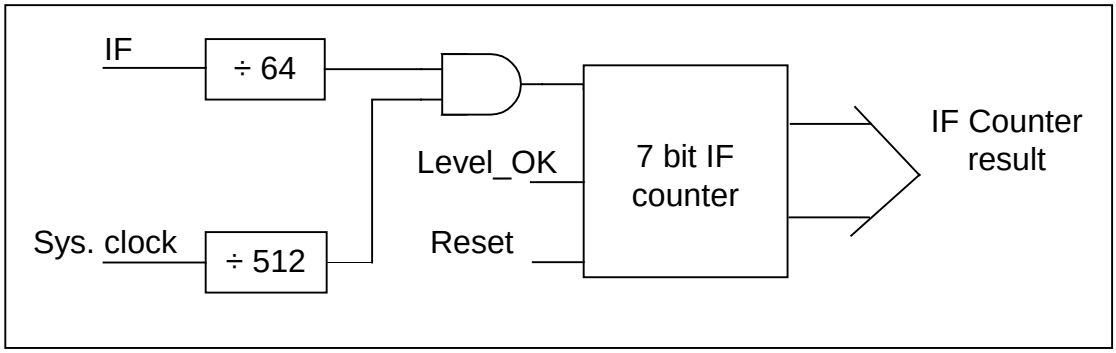


Figure 14: block diagram of IF counter

The counter result is also available via the bus. To read this result, the following actions will be taken:
- Write to bus
- After a write operation the result will be ready after 27ms. Wait until the result is available for the bus.
- Read the result.

Because the IF counter is not automatically updated, each time a read action is required, a previous write action must be performed.

At the end of the counting, the counter will be reset and a new cycle can be started again.

	Counter result	
IF input [kHz]	**F_{xtal} flag = 1**	**F_{xtal} flag = 0**
200	31	30
225	34	37
250	3F	3F

Table 3: counter result depending on the F_{xtal} flag

4.4 Level ADC

The level ADC block is an analogue to digital converter (ADC), which gives an indication of the fieldstrength of the RF input signal. This block is a four bits ADC, with 3dB resolution each bit. The level can be measured via the bus via bit 4, 5, 6 and 7 of data byte 4
A typical measurement of the level ADC is illustrated in Figure 15. The y-axis gives a decimal representation of the level ADC. The x-axis represents the RF input level, which is given in dBµV.

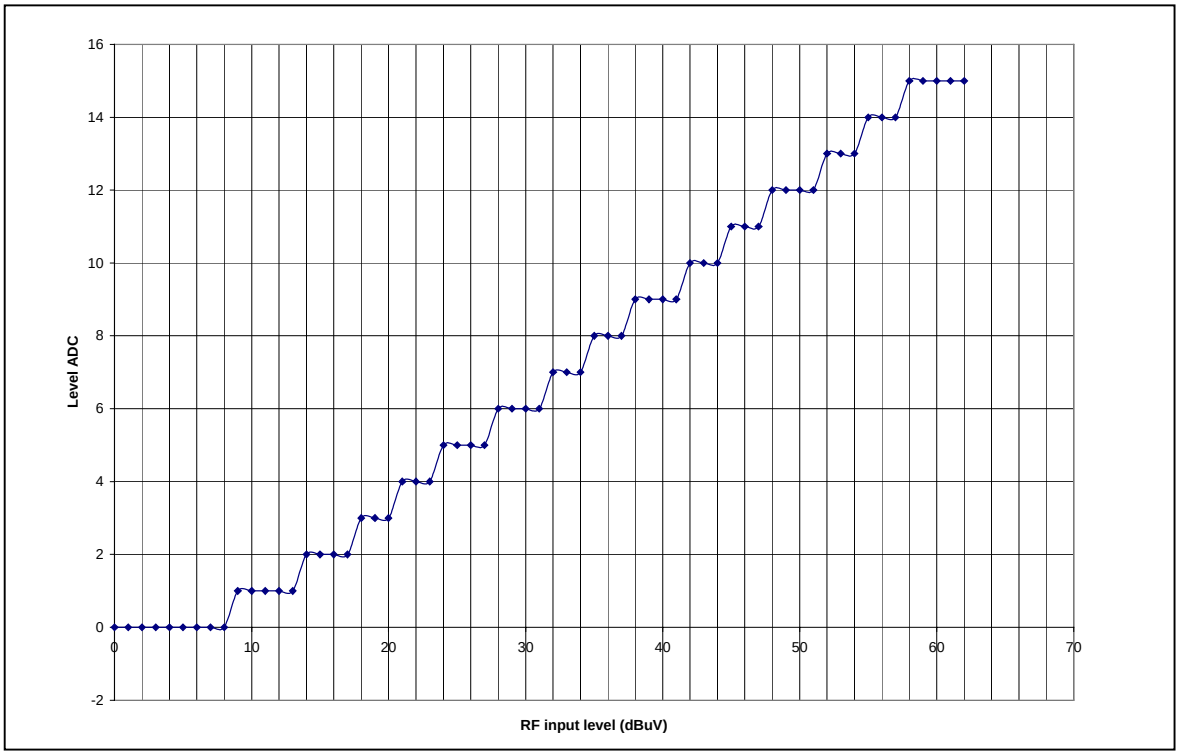


Figure 15: Level ADC input measured via the bus

A copy of the level ADC can be measured at TMUTE, pin 24. The impedance of this output is very high (about 400kΩ) and together with a capacitor (33nF) form a low pass filter, which filters the amplitude variations. This high ohmic output can only be measured using a very high input impedance device (e.g. FET or an OpAmp). The level ADC information at pin 24 is given with reference to the supply voltage.

Figure 16 gives a typical curve of the level ADC as a function of the RF input level (V_{cc}=2.7V)
Even when there is no RF input signal, the level output DC voltage is about 1,64V. From an input signal of 1.6µV (4dBµV) the level output rises linearly until it reaches a value of 2.1V at an input signal of 1mV (60dBµV). From then, the level output stays constant.

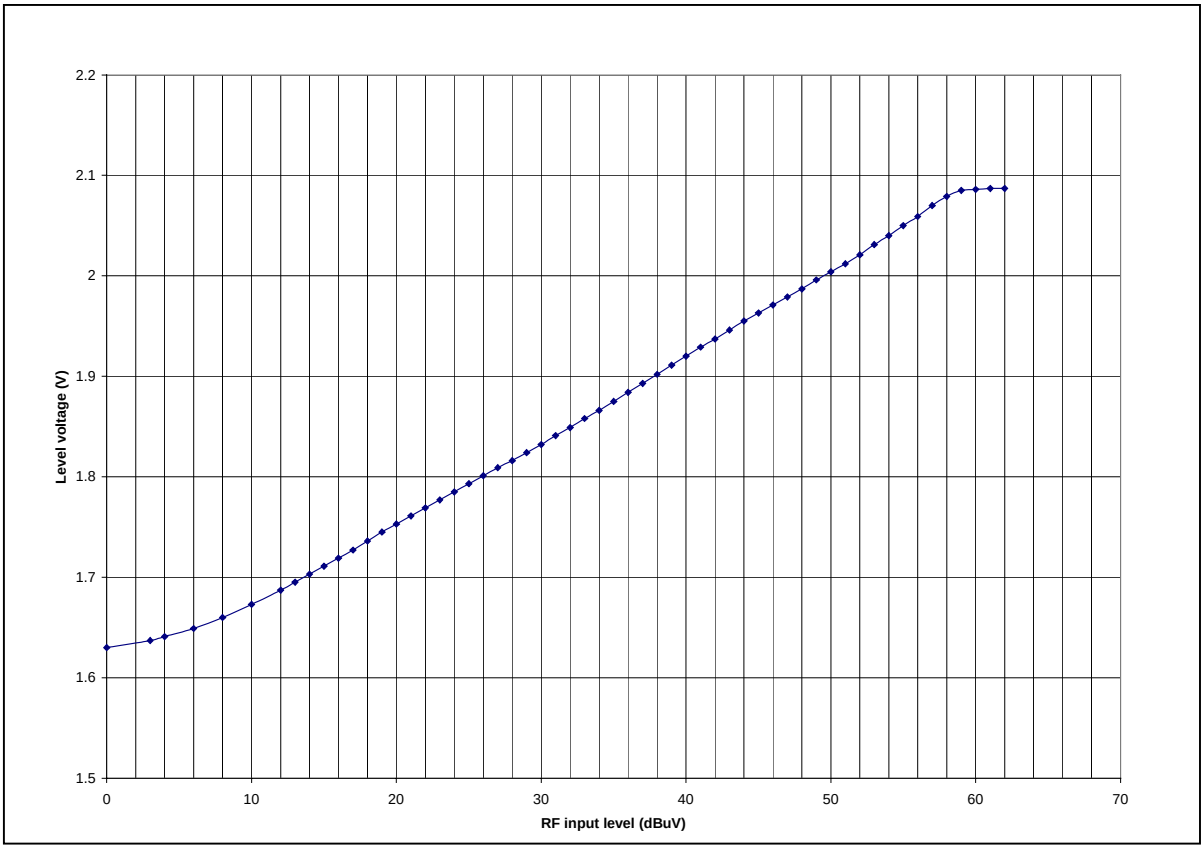


Figure 16: level ADC as function of the RF input level (V_{cc}=2.7V)

4.5 Tuning Algorithm

The tuning system can perform an autonomous search, or search can still be done in the classical way under µC control. When the tuner receives a (autonomous) search request (bit 6 of data byte 1 is set) it will begin scanning the FM band until a frequency is found or the band limit is reached.

High/Low side issues

As early discussed in this paragraph, the TEA5767/68 can be operated in two modes: High or Low side injection selectable with HILO bit (bit 4 of data byte 3) via the bus interface. Under certain circumstances is the selection of one of these modes not arbitrary. This is the case when high level signals are involved, as illustrated in Figure 17.

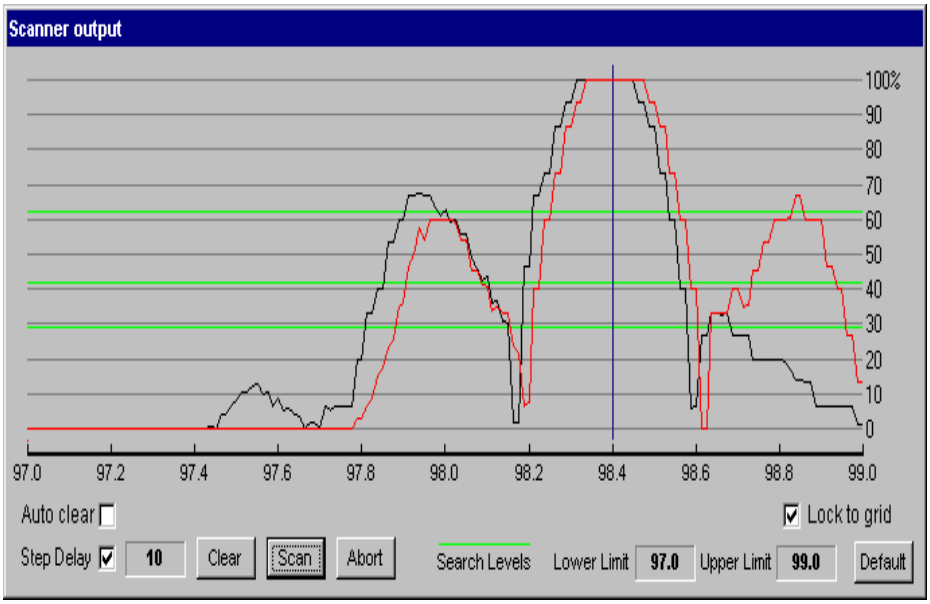


Figure 17: effect of high/Low side injection with strong signals

The wanted station is at 98 MHz at a signal level of 100 µV and there is a strong neighbouring station at 98.4 MHz with a signal level of about 2.5 mV. With HILO=1 (black curve) the image response of 98.4 MHz is right on top of the wanted station at 98 MHz, masking this wanted station. With HILO=0 (red curve) no interference is heard on 98 MHz. The image of the unwanted station can now be found at 98.85MHz.

In the demo software the following algorithm is used to set HILO to the optimal level:

Set HILO to “1”.
Tune to Fwanted + 450 kHz: measure signal level → LevelHigh
Tune to Fwanted – 450 kHz: measure signal level → LevelLow
If LevelHigh < LevelLow then HILO is “1” else HILO is “0”.

In the given situations no problems will arise with search tuning as the image frequencies are not on the search grid of 100 kHz.

However when the signal level of the wanted station increases to above about 3 mV false stops may be introduced due to unwanted mixing effects in the FM signal channel (see Figure 18).

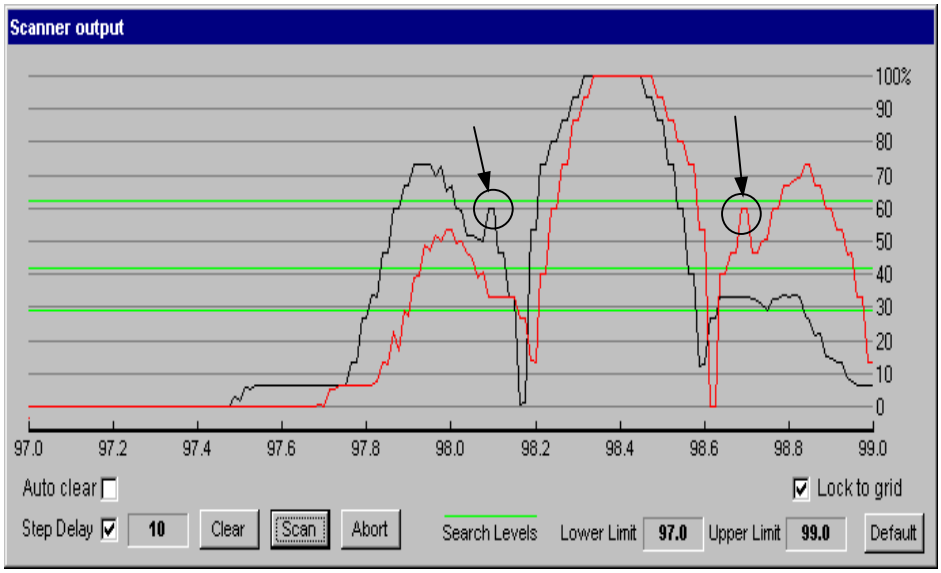


Figure 18: false stop by high level signals

Now two additional stops are introduced at 98.1 MHz (HILO =1) and on 98.7 MHz (HILO = 1) (see the circles around the signals in Figure 18).
In the demo software these stops are rejected with the following algorithm:

Measure the level when the search has stopped → Level 1
Toggle the HILO bit and measure level again → Level 2 and also read the IF counter result → IFC
Tuning is correct when the following formula is met:
Absolute value of (Level1 – Level2) < 2 and $31 < IFC < $3E

4.5.1 Preset mode

To tune the radio a wanted frequency the following actions will be taken:

First a PLL word has to be calculated. In paragraph 4.2.1 and 1, it has been explained how to calculate this word. If a high side injection is desirable the HILO bit is set to 1 otherwise 0. This information has to be sent to the tuner.
Other information can also be sent to set on/off the softmute (bit 3 of data byte 4), HCC (bit 2 of data byte 4) and SNC (bit 1 of data byte 4), etc

4.5.2 Search mode

To perform an autonomous search, MUTE and SEARCH bits should be set. At the same time the current frequency has to be increased or decreased with one grid step. The search direction and the stop level (see Table 4) can be chosen.

This information can be sent to the digital tuning and the control software must keep on reading until bit READY=1. In that case a station has been found or a band limit has been reached. In the last situation also the band limit flag is “High” (bit 6 of data byte 1in read mode). The software then has to wrap the frequency to the other band limit and initiates a new search action. At the end of the search action the MUTE bit should be set to zero again.
When a stop has been detected the HILO algorithm will be performed to check if the stop is valid and to find an optimum setting for the high/low side injection.

Bit 6 of data byte 3	Bit 5 of data byte 3	Field strength	Level_ADC
0	0	Not used	Don’t care
0	1	Low	0101
1	0	Middle	0111
1	1	High	1010

Table 4: search stop level

Care should be taken to prevent the algorithm ends up in an infinite loop when no station has been detected. This can be done either by lowering the search level or by exciting the loop when the band limit is reached for the second time.

N.B

*Because the tuning system is internally provided with 100kHz grid step, care should be taken when the tuner is clocked with the 32768Hz reference frequency. The grid step is then 98.304kHz (3*32768Hz).*
In that case, when performing a search and a station is found, the PLL word of the programmable divider will be read. The value of this word will be rounded and sent back to the tuner.

5 COMMUNICATION

The TEA5767HN can communicate with the external controller via an integrated on-chip bus interface. The tuner supports both I^2C and 3-wire bus interface, selectable via BUS MODE pin.
The bus interface is accessible via five pins. A typical I^2C interface application is given in Figure 19, and a 3-Wire interface is given in Figure 20.
The function of each pin is given below.

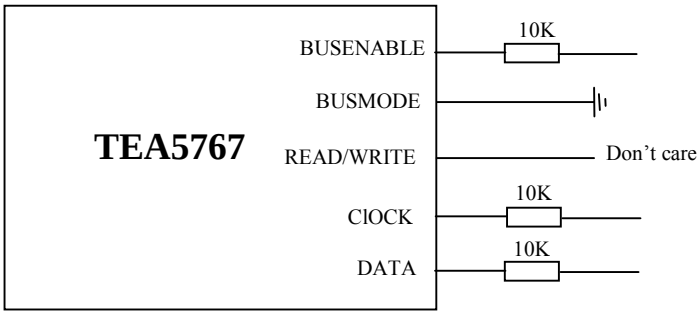


Figure 19 typical serial interface application with I^2C bus interface

BUS ENABLE (input)

The BUS ENABLE signal should be activated before any data transfer via the bus can be performed.
If the BUS ENABLE pin is LOW, the bus interface is deactivated. When the standby bit (bit 6 of data byte 4) is HIGH and the BUS ENABLE pin is LOW the standby current of the IC can be reduced below 10uA.

BUSMODE (input)

With this pin either the I^2C or the 3-wire bus interface can be selected. If the BUSMODE pin is connected to the ground the IC will operate with I^2C bus. If the BUSMODE pin is high 3-wire bus is selected.

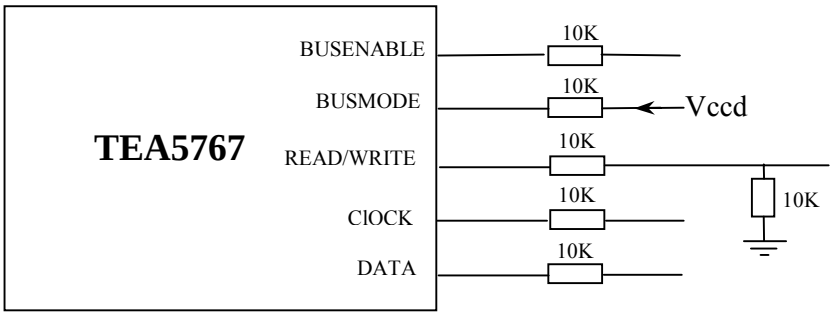


Figure 20 typical sieral application with 3-Wire bus interface

READ/WRITE (input)

A positive edge of the READ/WRITE pin enables data transfer in the IC. A negative edge at READ/WRITE pin enables the data transfer out the IC.
This pin is not used in I^2C mode.

CLOCK (input)

For clocking DATA in and out the shift register.

DATA (input/output)

The data input/output enables the data transfer from and into the IC.
The software can read valid data any time and without interrupting the search function. Writing data to the IC will interrupt the search function and the sent data will define the new status.
Care should be taken when continues reading is required, because the data on the output registers is not continue updated. Therefore each read action should be proceeded by a write action.

In the next paragraphs a brief description of I^2C and 3-Wire bus interface will be given.

5.1 I^2C bus interface

I^2C is a simple bi-directional bus interface. The bus requires only two lines, which are serial data (SDA) and serial clock (SCL). The bus is 8-bit oriented. Each device is recognised with a unique address.
The I^2C bus operates with a maximum frequency of 400KHz.

Data transfer to and from the TEA5767HN can begin when a start condition is created. This is the case if a transition from HIGH to LOW on the SDA line occurs while the SCL is HIGH (see).
The first byte transferred represents the address of the IC plus the data direction. A LOW LSB of this byte indicates data transmission (WRITE) while a HIGH LSB indicates data request (READ).
Each data put on the SDA must be 8-bits long (Byte) and each byte sent should be acknowledged by “ACK” bit. In case a byte is not acknowledged, the transmitter should generate a stop condition or restart the transmission.

At power on, the mute bit (bit 7 of data byte 1) is set. All other bits are set to low. To initialise the IC all bytes should be transferred. If a stop condition is created before the whole transmission is completed, the remaining bytes will keep their old setting. In case a byte is not completely transferred, the new bits will change their setting but a new tuning cycle will not be started.

The transfer of data bytes should be ordered from low to high. First the address then byte 1, byte 2, etc. The MSB of each byte will be send first.

The IC address is 1100000. This means that the first byte to be transmitted to the TEA5767HN should be “C0” for a WRITE operation or “C1” for READ operation.

A transmission can be terminated by generating a stop condition. This is the case when the SDA goes from LOW to HIGH while the SCL is HIGH.

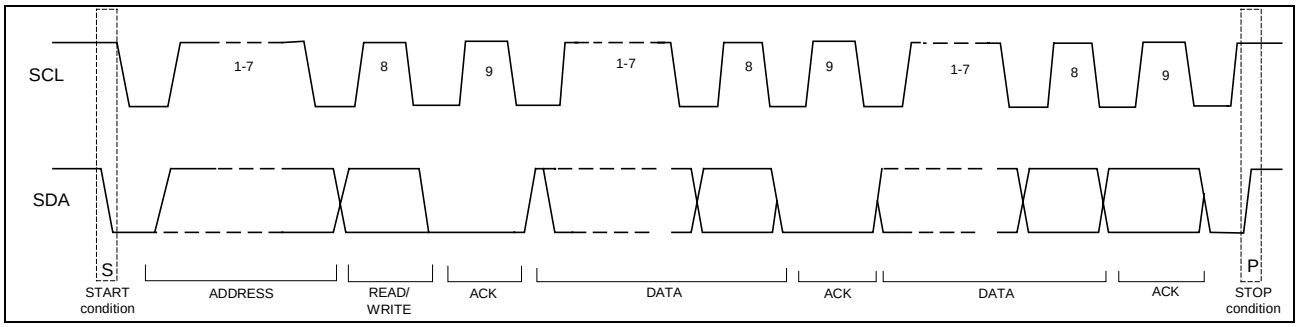


Figure 21 data transfer from and to TEA5767HN

5.2 3-Wire bus

3-Wire bus is a serial interface with 3 lines: WRITE/READ, CLOCK and DATA. The bus operates at a maximum rate of 1MHz.

With the WRITE/READ line the direction of the data can be selected. A negative edge at this pin enables data transfer out the IC. While a positive edge of WRITE/READ pin allows data to be written to the IC. The WRITE/READ pin should change only if the clock is LOW.

At power on, the mute is the unique bit, which is set. All other bits are random. To initialise the IC all bytes should be transferred.

Write mode

A positive edge the WRITE/READ signal indicates that data can be transmitted to the IC. During the next clock pulse data must be stable. Data may change only if the clock is LOW.
At rising edge of the clock data will be shifted in the register.

The data transfer can be terminated by setting the WRITE/READ pin. This is possible after sending two bytes of the new tuning information or after each following byte.

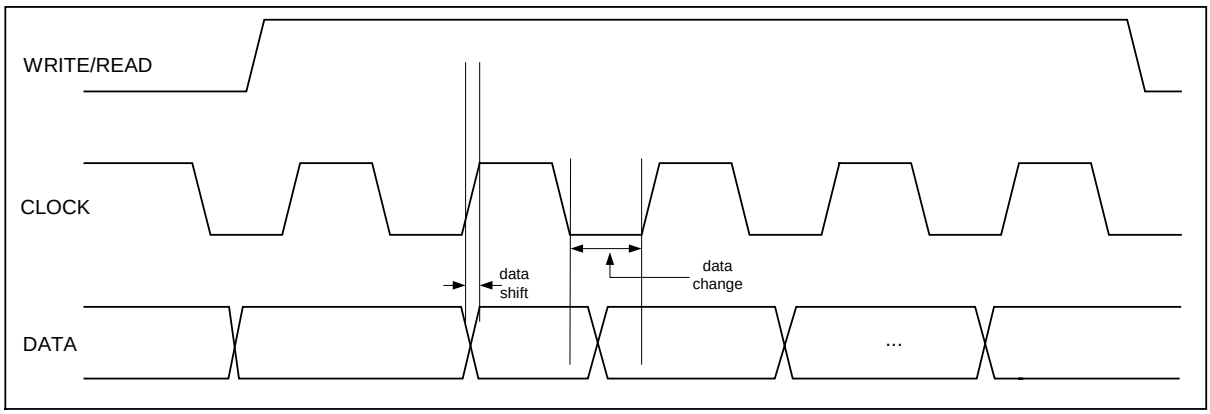


Figure 22 write action in 3-Wire bus interface

Read mode

A negative edge of the WRITE/READ pin indicates that the μ-controller wants to read data from the IC. The WRITE /READ pin must change only if the clock is LOW.
At rising edge of the bus clock data is shifted out the register. This data is available from the moment that the clock is HIGH until the following rising edge of clock.

During the positive edge of the clock, data must be stable.

Setting the WRITE/READ pin HIGH will terminate the read action.

Prior to a read action a write action is required in order to update the read register content.

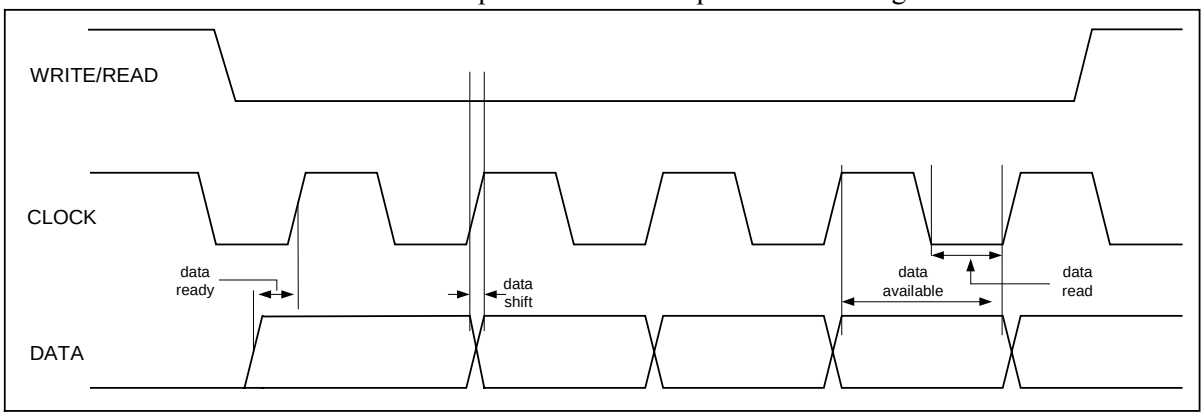


Figure 23 read operation in 3-Wire bus interface

6 TEA5767HN APPLICATION

The TEA5767HN has a simple application with a few external components. This application comprises two major circuits: the RF input circuit and the FM VCO circuit (see Figure 2).

In this paragraph the TEA5767HN application will be described.

6.1 RF input

The antenna-input signal is fed into the balanced FM-RF inputs (pin 35 and 37) via a RF matching impedance circuit. A series capacitor, two parallel capacitors and a coil (L1) build this circuit. The coil used in this circuit should have a minimal Q factor of 30. Its tolerance is ± 5%.
Together with the impedance of the LNA, the RF matching circuit forms a low Q band pass filter

In order not to affect the sensitivity of the receiver, the circuit can be optimised to match the antenna impedance. Figure 24 gives a typical matching circuit for 40Ω source impedance. The frequency response of this circuit is given in Figure 25.

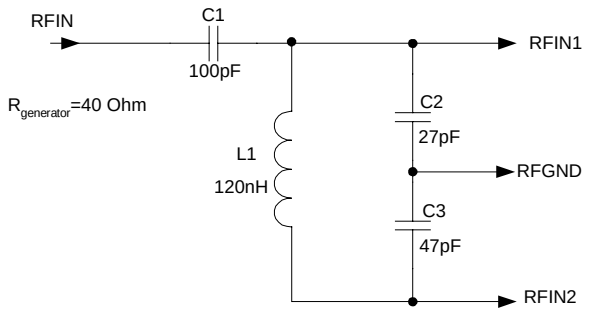


Figure 24 Antenna matching circuit for 40Ω source impedance

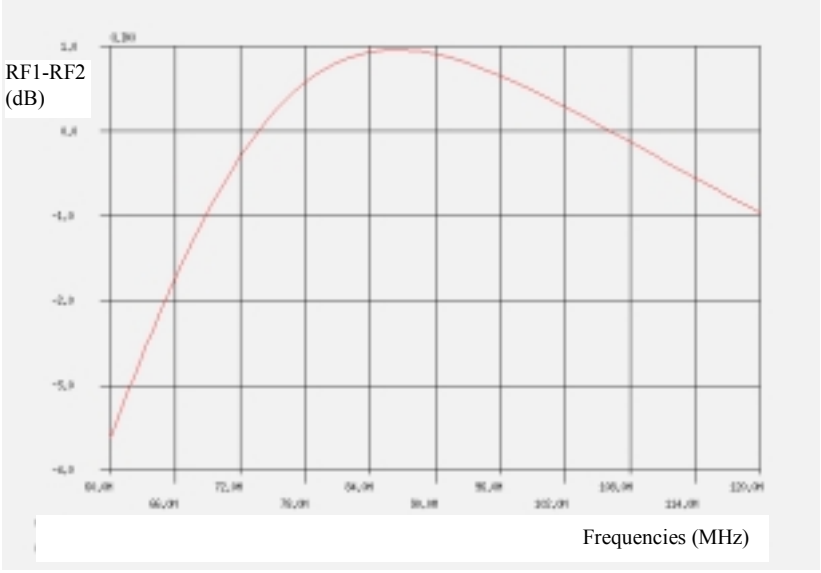


Figure 25 Frequency response of the matching circuit in figure 24

Figure 26 gives an example of a matching circuit for 75Ω source impedance. The frequency response of this circuit is given in Figure 27

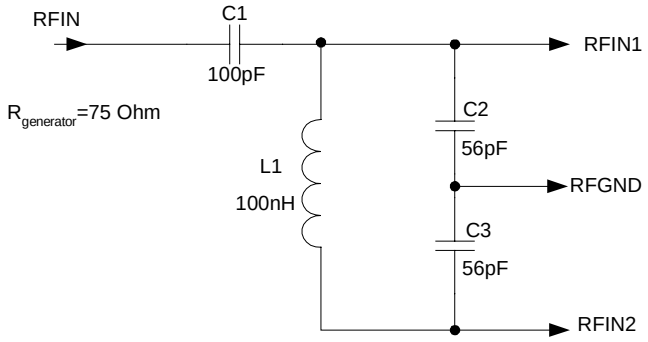


Figure 26 Antenna matching circuit for 75 Ω source impedance

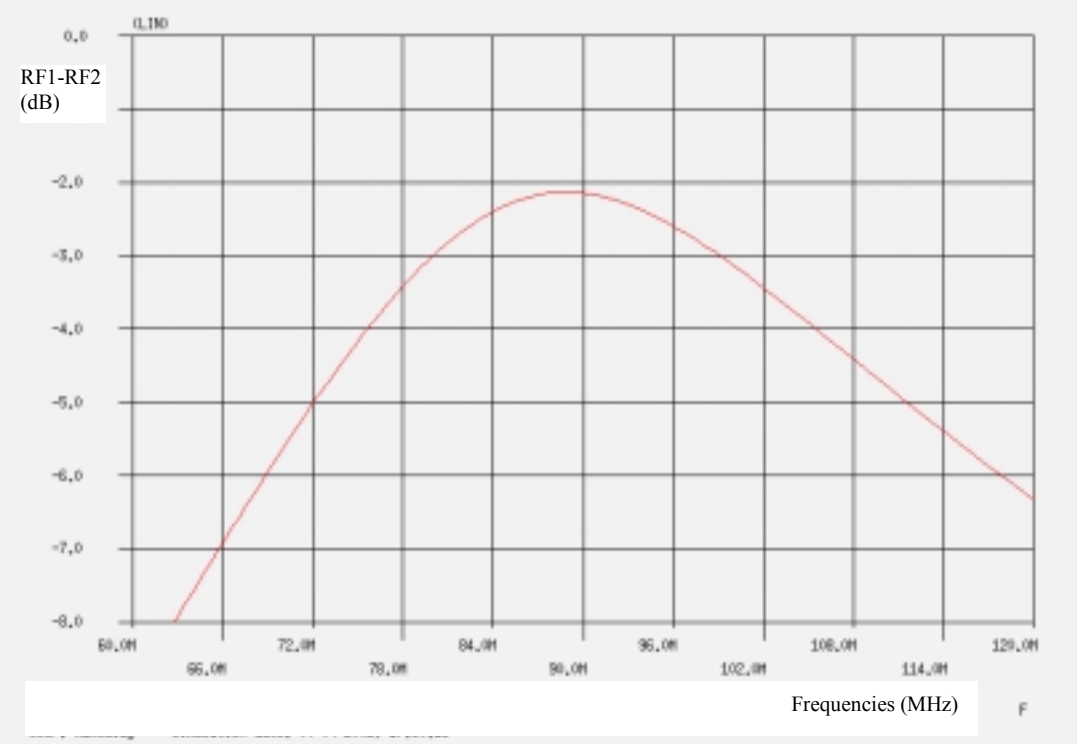


Figure 27: frequency response of the matching circuit of figure 26

6.2 VCO tank circuit

The VCO circuit produces a signal at double frequency necessary for the tuning system. A divider will half the frequency of this signal and then deliver it to the PLL.

In the proposed application the used tuning diodes D1 and D2 are BB202**.** This ultra small diode is fabricated in planar technology. It has a low series resistance (0.8Ω maximal), which is very important for the signal to noise ratio (SNR). In Figure 28, the capacitance value of this diode is given as function of the reverse voltage.
In our application proposal these diodes can tune the complete FM band (71-108MHz) with less then 3V-supply voltage. The minimum voltage at pin 34 (V_{CC}) should be 2.5V and the maximum voltage 5V. Inside the IC a chargepump is responsible for delivering the required current to charge/discharge the external loop capacitor. During the first 9 ms the charge pump delivers a fast current of 50uA. After that this current is reduced to 1uA.

In the given application the typical tuning voltage is between 0.54V (2*108MHz) and 1.57V (2*87.5MHz).

The minimum voltage to frequency ratio, often referred to VCO conversion factor (K_{vco}), is thus about 40MHz/V. The oscillator circuit is designed such that the tuning voltage is between **0.2V and V_{cc}-0.2V**. In order to match the VCO tuning range two serial coils L2 and L3 are put in parallel with the tuning diodes D1 and D2. A typical FM oscillator-tuning curve, using BB202 tuning diodes, is given in
Figure 29.

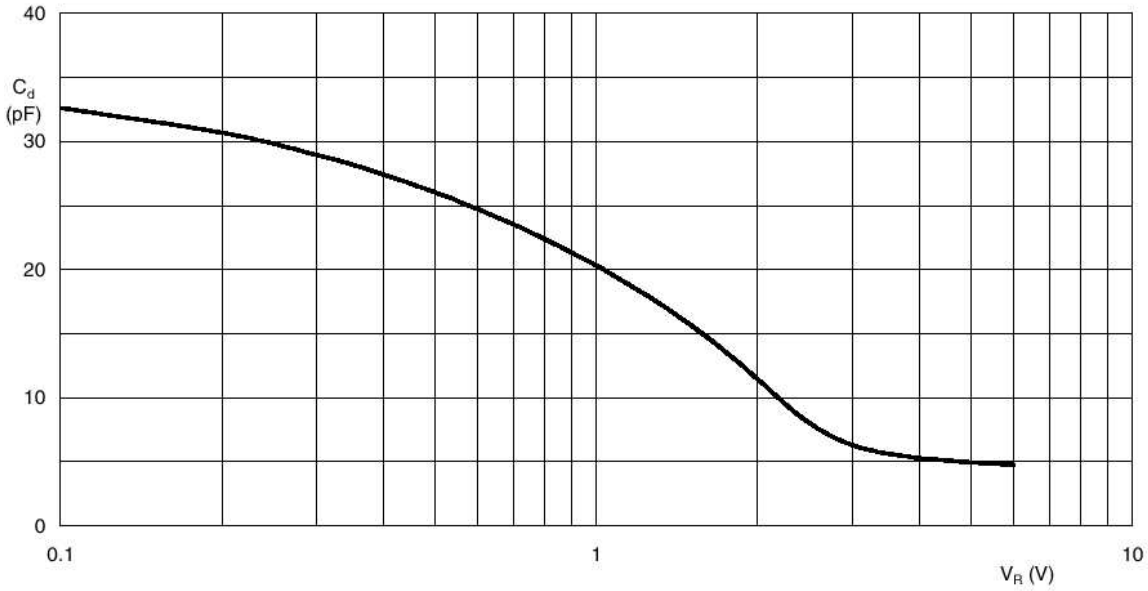


Figure 28 Diode capacitance as function of reverse voltage; typical values

The inductance value of the oscillator coils L2 and L3 is about 33nH (Q=40 to 45). The inductance is very critical for the VCO frequency range and should have a low spread (2%). The quality factor Q of this coil is important for a large S/N ratio figure. The higher the quality factor the lower the noise floor VCO contribution at the output of the demodulator will be. With a quality factor between 40-45 a good compromise can be found between the size of the coil and the, by the oscillator determined, noise floor.

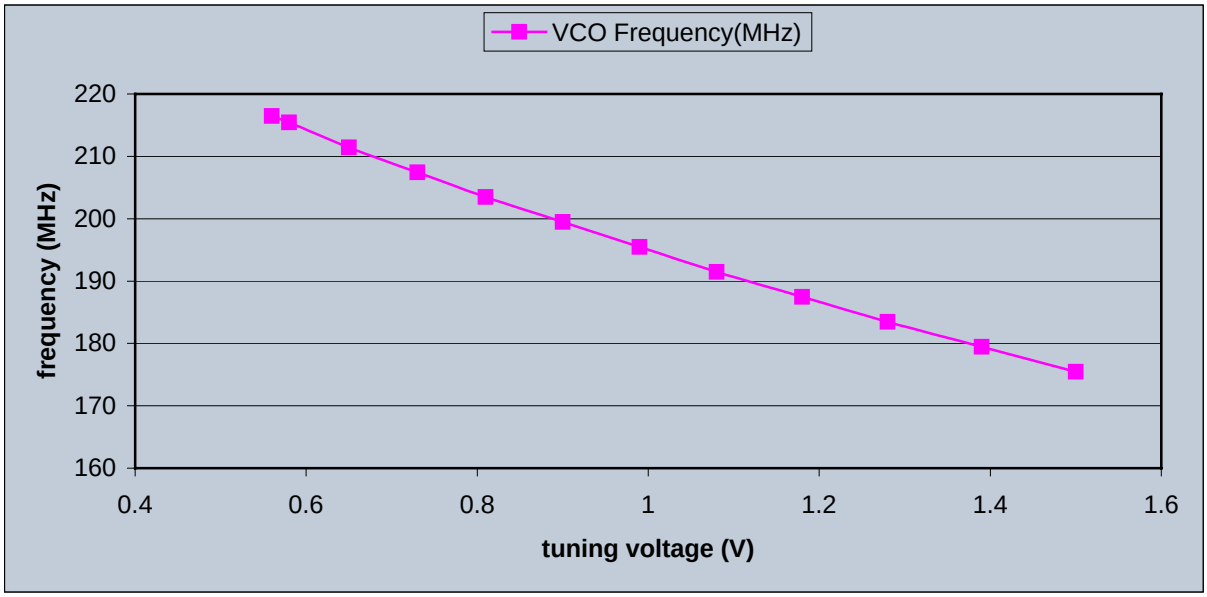


Figure 29 typical oscillator tuning curve of proposed FM application

6.3 Reference frequency

The TEA5767/68 can work with two crystal clocks: 13MHz or 32768 Hz. The synthesiser can also be clocked with 6.5MHz via the Xtal2 pin. It is also possible to use an external 32768Hz, a 6.5MHz or a 13MHz reference signal. This can be connected via the Xtal2 pin.

6.3.1 Internal clocking

Figure 30 gives a possible connection of the crystal clocks to the tuner.

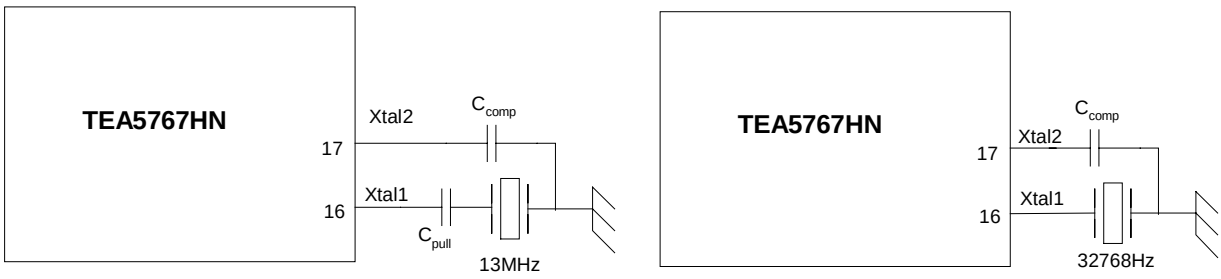


Figure 30 connection of the 13MHz and 32768Hz crystal to the tuner

When using a 13MHz crystal clock this should have a frequency deviation of ±20 ppm. Its shunt capacitance must not exceed 4.5pF and the series resistance is maximal 100Ω. The temperature drift should be in the order of ±30 ppm over a temperature range of –40°C to +85°C.

In the TEA5767HN and TEA5768HL demo boards a 13MHz crystal oscillator is used. This is a surface mount type, NX4025GA. The specifications of this crystal are given in Table 5.

Nominal frequency	13MHz
Overtone	Fundamental
Frequency Tolerance	± 10 ppm at 25±3°C
Temperature characteristics (in reference to +25° C)	±15 ppm (-30 ~ +85°C) For mobile communication equipment ±15 ppm (-10 ~ +60°C) for computer, OA product
Pull Capacitance	7 ppm /pF (at 13pF) Typical
Equivalent Series Resistance	60Ω
Drive Level	10μW (100μW max)
Standard Load Capacitance	13pF
Operable Temperature Range	-30 ~ +85°C

Table 5: specification of NX4025GA 13MHz crystal

The choice of 32768Hz reference frequency makes it possible to use a cheap 32.768kHz watch crystal. A drawback of these clocks is that they have a very high second order temperature coefficient. This may result in de-tuning the radio or a search action may fail.
Care should be taken when using this crystal. The accuracy of the 32768Hz crystal can be checked by tuning the radio to 81.4 MHz with high/low side injection and reading the IF via the bus. The IF must be 37Hex.

An other issue when using this crystal is the grid position. It is not possible to create a 100kHz grid position, but 98.304kHz (3*32768Hz). This should not be a problem if this is resolved in software.

The motional capacitance of the 32768Hz crystal should be between 1.5fF and 3fF. Shunt capacitance must be max 3.5pF. The series resistance should not exceed 75KOhm.
Further, the frequency accuracy of this crystal must not exceed ±20 ppm, while the temperature drift should be in the order of ±50 ppm over a temperature range of –10°C to +60°C.

6.3.2 Pulling and compensation

The 13MHz crystal can be pulled using a proper capacitor (C_{pull} at pin 16 in Figure 30). A capacitor can also used to compensate the clock (C_{comp} at pin 17 in Figure 30). In our application with XN4025GA, C_{pull} Is equal to 1pF.

The 32768Hz clock should not be pulled. If necessary, a compensation capacitor can be added as given in Figure 30.

6.3.3 External referance

The TEA5767HN can be clocked externally with 32768Hz, a 6.5MHz or a 13MHz reference signal. This can be connected via the Xtal2 pin. Xtal1 (pin 16) stays open.

The external signal should be a square wave with a duty cycle of 20 a 80%. The connection of a 13Mhz external signal is given in Figure 31.

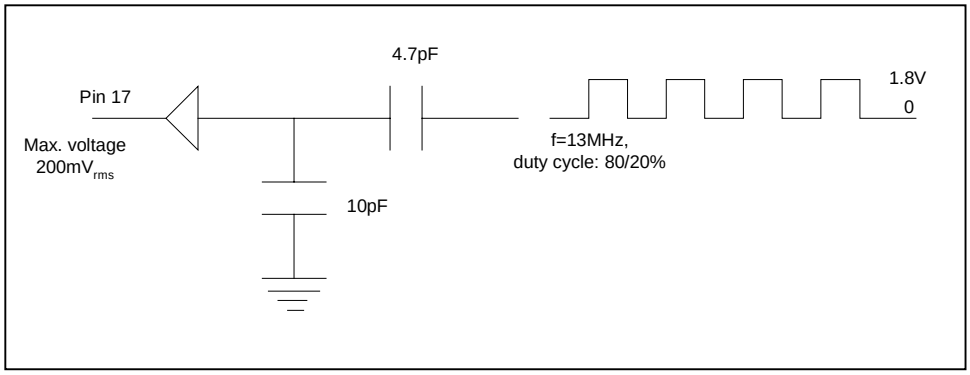


Figure 31 connection of 13Mhz external signal

Figure 32 ilustrate the connection of a 32768Hz external signal to the TEA5767HN.

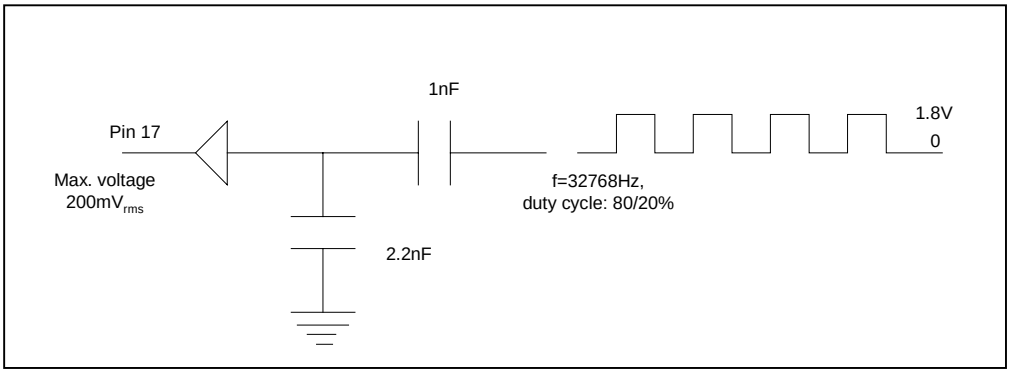


Figure 32: connection of 32768Hz external signal

6.4 Layout Hints

It's important to keep the track between the oscillator coils and pin3 and 4 of the TEA5767HN (pin 2 and 3 for TEA5768HL) as short as possible. Each millimetre track adds 1nH extra inductance to the wanted inductance value. This may influence the tuning range and can also lead to wrong oscillation frequencies. For the same reason it's also important to have a short return track (ground) which has also some isolation between OSC ground and RF ground.
Any additional current must be kept away from the loop filter and VCO signal pad.
All other ground pins should be connected to the groundplane. It is preferable to have groundplanes on both PCB sides. Use as much as possible ground vias for lowest groundplane impedance. To get the highest possible quality factor it's important to connect the top of the coil to the signal track. No groundplane should be used below the coils.

7 RDS/RBDS

The FM stereo radio can be extended with a RDS/RBDS function. The SAA6588 is a one-chip solution with a combined RDS/RBDS demodulator/decoder. The supply voltage is specified between 4.5V and 5.5V. This supply voltage is necessary to guarantee all specifications.
The motherboard developed for the TEA5767/68 is ready to be supplied with the SAA6588 chip.

The input signal for the RDS/RBDS demodulator is supplied by the TEA5767/68 radio IC via the MPX output signal. This signal is available at pin 25 for the TEA5767HN and pin 20 for TEA5768HL. The MPX output has high impedance so that it can not directly connected to the RDS input. In the motherboard this signal is first buffered via a transistor (BC859B) and then connected to the RDS chip. Further a low pass filter is used to remove undesired IF components from the MPX signal.

In the next sectionSAA6588 is briefly described.

7.1 RDS/RBDS with SAA6588

The RDS/RBDS pre-processor SAA6588 is a CMOS device that integrates all relevant functions in one chip. The pre-processed RDS/RBDS information is available via the I^2C-bus. The demodulator of the SAA6588T contains a band pass filter with a centre frequency of 57 kHz. This filter extracts the RDS/RBDS sub-band from the MPX signal. This signal will then be digitised for further processing by the digital demodulator. This will perform symbol decoding, block synchronisation, error detection and error correction.
The SAA6588 has also additional detectors for multi-path, signal quality and audio signal pauses. In this application, these detectors are not used. The block diagram of the SAA6588 concept is given in Figure 33.

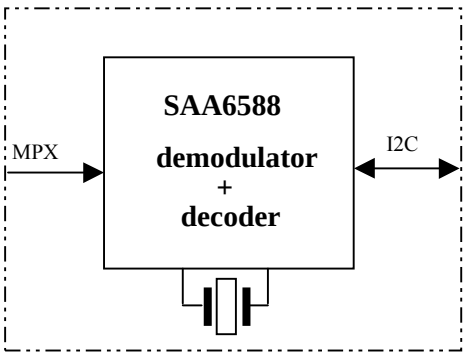


Figure 33 connection diagram of the SAA6588

The pre-processor of the SAA6588 handles the complete processing and decoding stream from the demodulator. The SAA6588 has different data processing modes, which are software programmable via the bus.

For further information about the SAA6588 a data sheet (SAA6588) and an application note (AN99005) are available.

8 AUDIO AMPLIFIER

The audio output level of the TEA5767/68 radio IC is not sufficient to directly drive a speaker or headphone. A digital volume control is also not available. The Philips Semiconductors audio group has developed an audio amplifier for small sized and low power applications. This IC is called TDA7053 and is available is SO16 or DIP16 package. In the proposed application this amplifier is used. This stereo audio amplifier can deliver 2 x 0.125W BTL into 16Ω load using a 5V-power supply. A Missing Current Limiter (MCL) is build-in. This circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA. This level of 100mA allows for headphone applications (single-ended)

The TDA7053 has a DC volume control. In order to control the volume of this amplifier via software a digital to analogue converter (DAC) is necessary. For this purpose a simple 4-bits DAC is used which is constructed by means of resistors. To make the volume control independent of the supply voltage, HEF4066BT is used as a switching device. This IC has four independent bilateral switches and now the resistors can be connected to a stabilised voltage (see Figure C1, Appendix C).

Using the demo software four volume control signals can be generated direct with the Dual Single Master interface (PR37156). Each pin can be set to a logic “1” or “0”. These signals are connected to the DAC, which will delivers a DC signal. This voltage is maximal (1.2V) when the four DAC inputs are low (Bit 0=0, Bit 1=0, Bit 2=0, Bit 3=0). In case these signals are high the DAC output will be minimal (0.60V) (see Table 6). The DAC output is directly connected to the DC volume control 1 and 2 of the amplifier.

The maximum gain of the amplifier is 40.5 dB (the control range is 73.5dB typical) and can be selected between -33dB and 40dB with DC volume control 1 and 2 at pin 2 and 8.

Bit 3	Bit 2	Bit 1	Bit 0	DC volume control ½ (Volt)	Gain (dB)
0	0	0	0	1.2	40
0	0	0	1	1.16	38
0	0	1	0	1.12	37
0	0	1	1	1.08	36
0	1	0	0	1.04	34
0	1	0	1	1.00	32
0	1	1	0	0.96	28
0	1	1	1	0.92	24
1	0	0	0	0.88	20
1	0	0	1	0.84	16
1	0	1	0	0.80	12
1	0	1	1	0.76	8
1	1	0	0	0.72	4
1	1	0	1	0.68	0
1	1	1	1	0.64	-4
1	1	1	1	0.60	-8

Table 6 Volume control

9 INSTALLATION GUIDE

An evaluation demo package will contain the following boards and cables

- Dual Single Master 3Wire/I2C interface PR37156 (parallel printer port interface!)
- motherboard PR73002
- one of the following modules TEA5767HN, TEA5767HL or TEA5768HL demo board
- two times (0.5 meter) four wire flatcable (1 on 1)
- one time (0.5 meter) nine wire flatcable (1 on 1)
- one time (1 meter) three wire flatcable with black, green and red supply connector

The next paragraphs explain how to install the hardware and software in order to demonstrate the operation of the tuner board.

9.1 Hardware

Figure 34 gives an overview of the board's interconnection.

Figure 34 connection of TEA5767/68 demo board

The installation procedure is the same for the three boards and can be performed as follow:

- Place the FM Stereo demo board on to the motherboard PR73002 at position P2, P3 and P4 as shown in Figure 34 and Figure 35 at positions P2, P3 and P4.
- Connect the motherboard PR73002 with 3 separate cables to the I^2C-interface PR37156 (P5, P6 and P7 of PR73002 to respectively P2, P1 and P3 of PR37156)
- Connect the supply voltage cable to P8 of PR73002, the red banana plug to a voltage source of +5V, the green plug to a voltage source of +2.7V and the black one to ground.
- Connect the sub-d 25 pins connector of PR37156 to a free parallel port (LPT) of a PC.
- Connect a FM antenna to the SMB connector P1 of the demo board.
- Connect an audio amplifier or any other measurement device to one of the audio output connectors P10, P11, P9 (Audio_L, Audio_R, MPX) or a headphone to P12 (Amp_Audio).

- Start the control program **TEA5767**, as explained in $9.2.

In Figure 35 is the interconnection between the DSM bus interface and the motherboard given

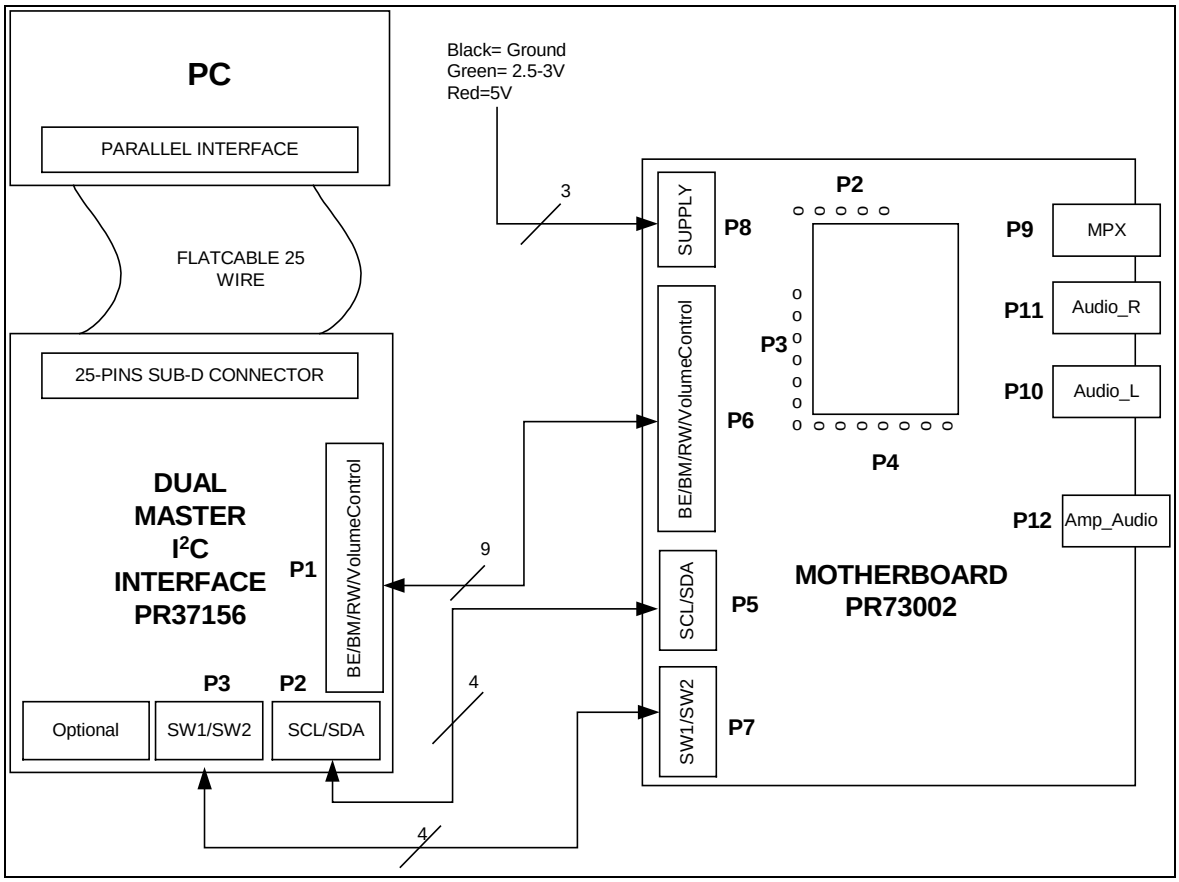


Figure 35 connection of the DSM interface to the motherboard

NOTES:

Make or check the interconnection according to the schematic drawn below. The demo boards should work at 2.7V and the I^2C, the amplifier and the RDS decoder at 5V.

The maximum supply voltage is 5V !!!!!

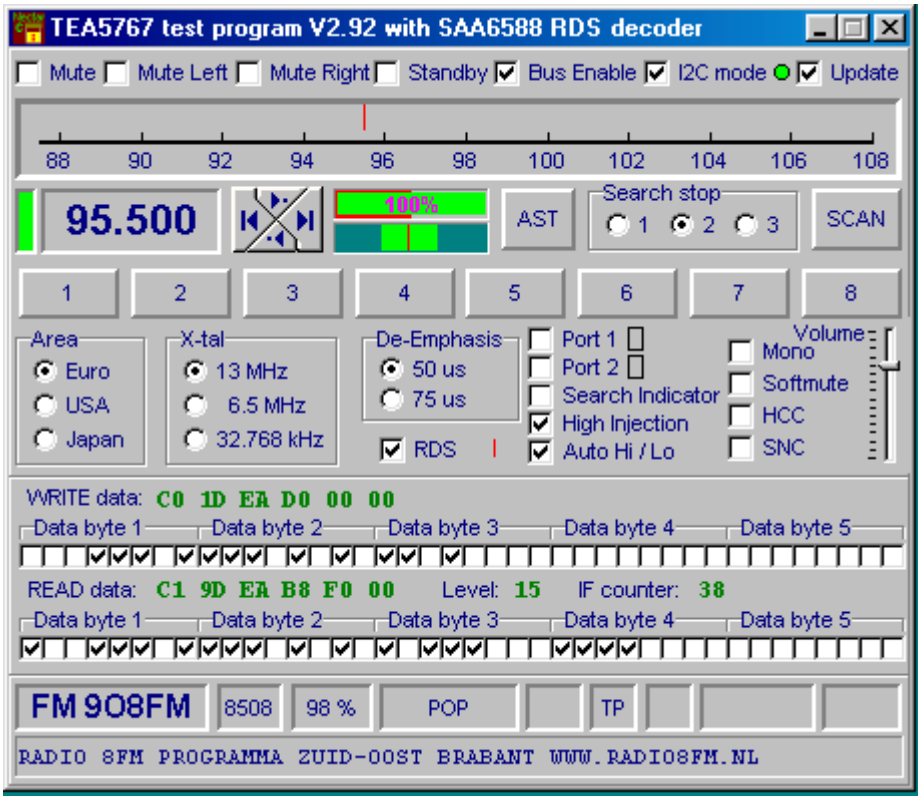
All cables should be connected between DSM interface and motherboard. The software will automatically detect whether a RDS module is present at start-up.

9.2 Software

Before the software is started please check that the hardware is connected and supplied according to the interconnection diagram of chapter 9.1. The software program TEA5767 can be used to control the TEA5767HN, TEA5767HL and the TEA5768HL, irrespective of the presence of an RDS IC or not.

This Windows based program is written in Delphi 1.0 and will work with Windows95/98 operating system and Windows NT

The TEA5767rds.exe file contains also the necessary I^2C drivers for the operating system. Just start the file and follow the instruction.
After the installation procedure, the TEA5767 control program can be started. The main window (shown below) will appear. In the example below the RDS is active.



The program will automatically detect the presence of the RDS module. The main window contains now an extra part (the two lower lines) reserved for the RDS information. When the PR37001 mother is used without RDS, the window will only show the upper part and the lower two RDS display lines will be skipped.

The software should be re-initialised when the supply voltage is switched on/off during program execution. This can be done by a double-click on the initialisation button (red circle). The user interface is quite intuitive. For most of the buttons and functions a short description will show up as soon as the mouse pointer is close to it. The RDS/RBDS functions are also described, but for those who are not so familiar with RDS/RBDS a short explanation of the RDS items (shown above) is given:

- FM908FM – this is the PS (Program Service Name)
- 8508 – this is the hexadecimal PI (Program Identification) code
- 98% – this gives an indication of the RDS/RBDS quality
- POP – this is the PTY (Program TYpe) information
- STEREO – decoder information from RDS/RBDS (not shown on the display)
- MUSIC – the music/speech flag (not shown in the display)

- EON – this station supports EON (Enhanced Other Networks) (not shown on the display)
- TP – indicates that the actual station can transmit traffic information TP (Traffic Program)
- TA – when TP is also active: a traffic announcement is active
  when TP is inactive: through EON the radio "knows" where Traffic Announcement can be found

- Example: RADIO 8FM PROGRAMMA ZUID-OOST BRABANT WWW.RADIO8FM.NL – Radio Text

10 SPECIFICATIONS

The FM radio and RDS performance is measured on a few representative demoboards. The characteristics are only indicative and could definitely not be guaranteed because of the limited number of measured samples. A typical FM performance curve of the TEA5767HH is given in Figure 36 (see page 47).

10.1 FM radio + RDS characteristics

Condition: V_rad=2.7V, Tamb = 25° C, F_{tun}= 98 MHz, F_{dev} = ± 22.5kHz, F_{mod} = 1 kHz

	TEA5767HN/TEA5767HL/TEA5768HL
Supply voltage	2.5V min and 5Vmax.
Total supply current	15mA
Tuning voltage	0.2 ↔ (V_{ccosc} –0.2)V
(S+N)/N = 26 dB	1.3 µV
-3 dB point	1.1 µV
S/N at 1mV (max)	58 dB
Image rejection	30 dB
Stereo separation (1kHz)	30 dB
THD distortion f_{dev}= ±75 kHz	< 1%
RDS sensitivity for 100% Correct blocks f_{dev}= ±2 kHz	10 µV

Table 7: FM radio + RDS characteristics

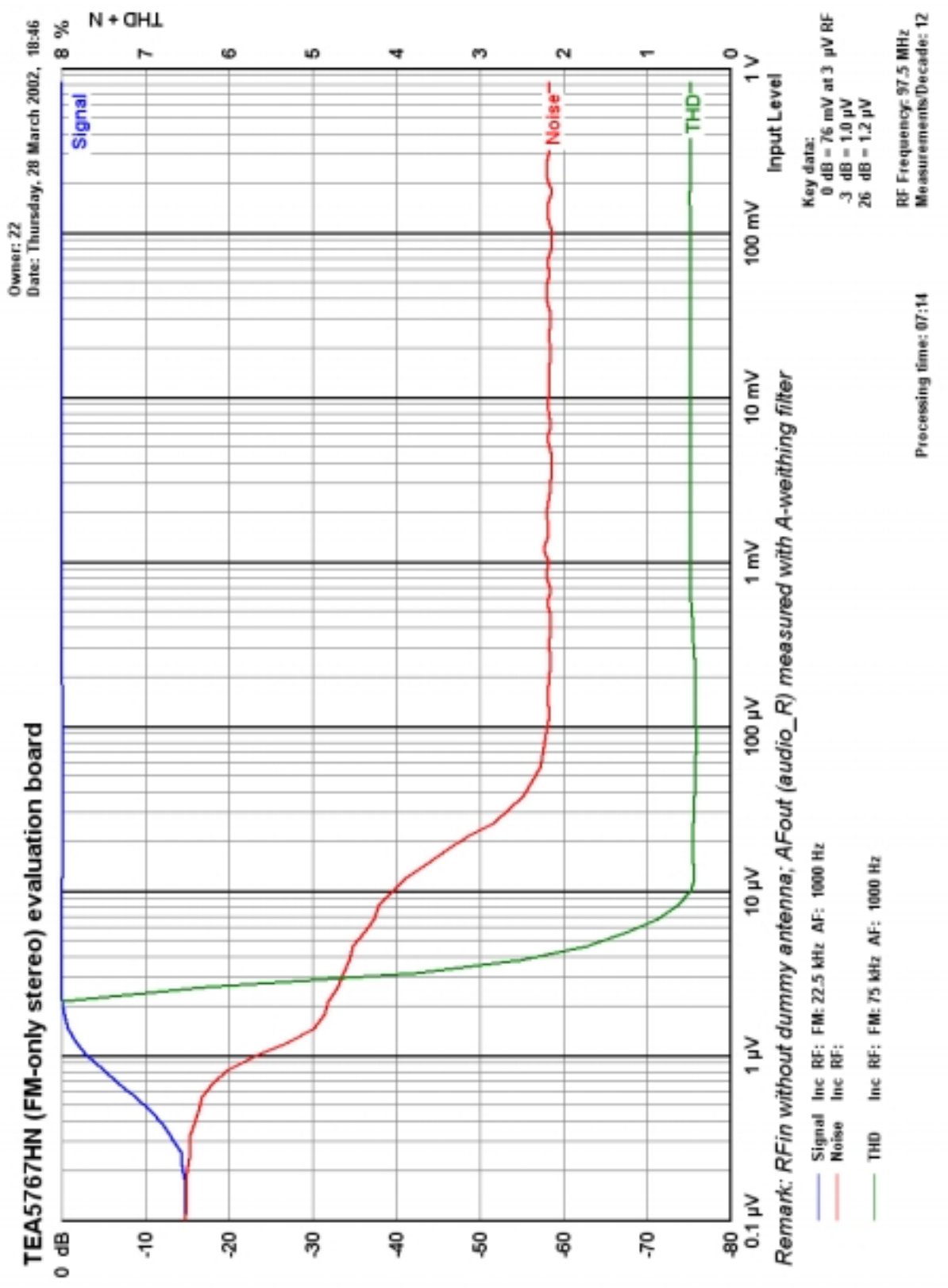


Figure 36 FM characteristic of TEA57567HN demo board

APPENDIX A: TEA5767HN DEMO BOARD (HVQFN40 FM-ONLY STEREO)

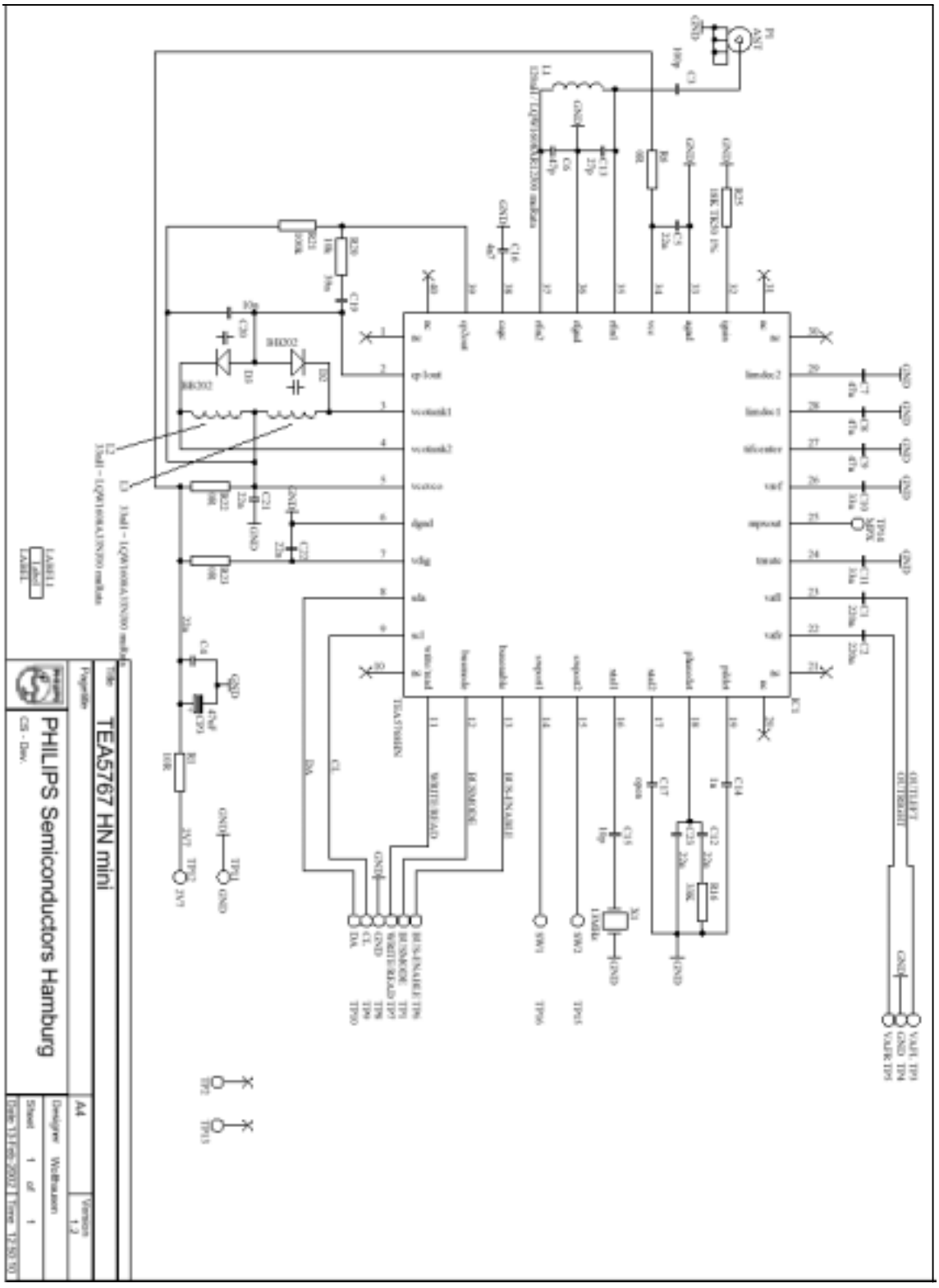


Figure A-1 SCHEMATIC TEA5767/68HL demo board

APPENDIX A: TEA5767HN DEMO BOARD

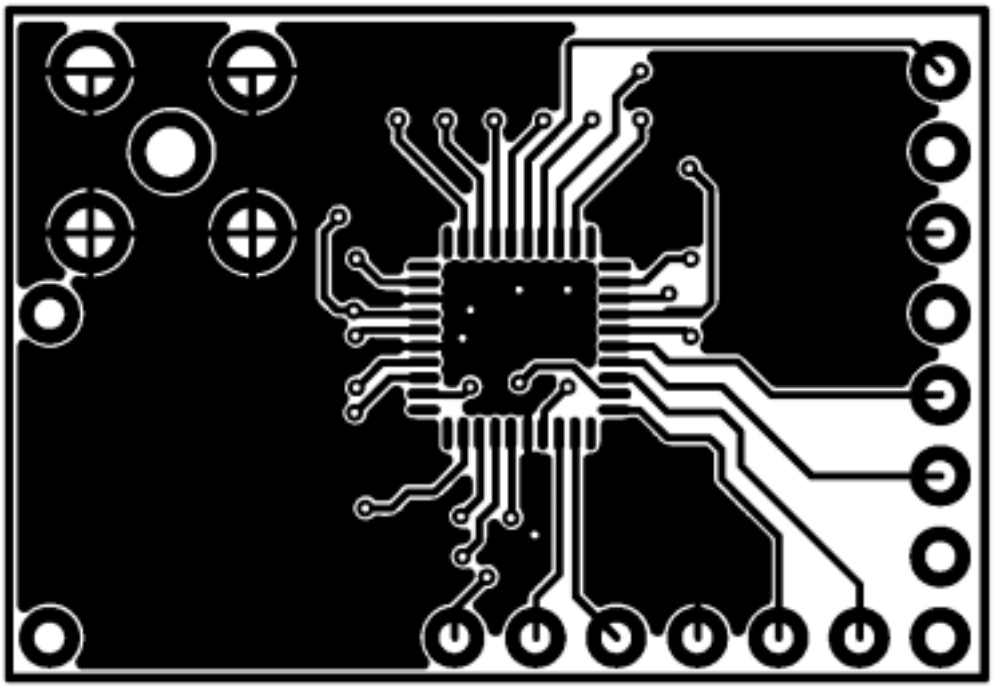


Figure A-2 REFERENCE TOP TEA5767HN demo board

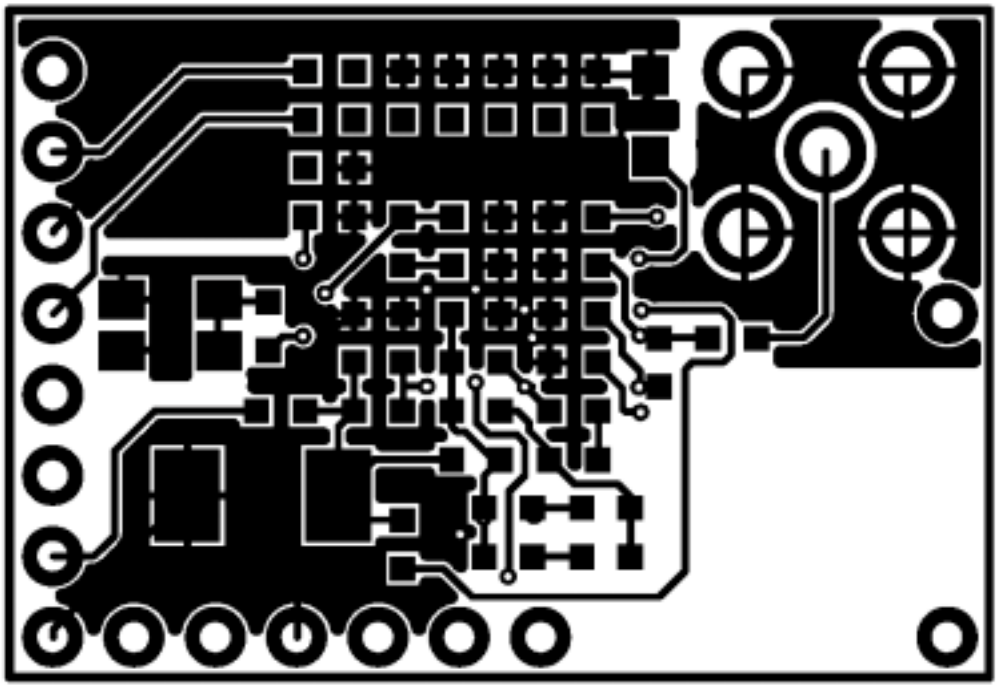


Figure A-3 SIGNAL TOP TEA5767HN demo board

APPENDIX A: TEA5767HN DEMO BOARD

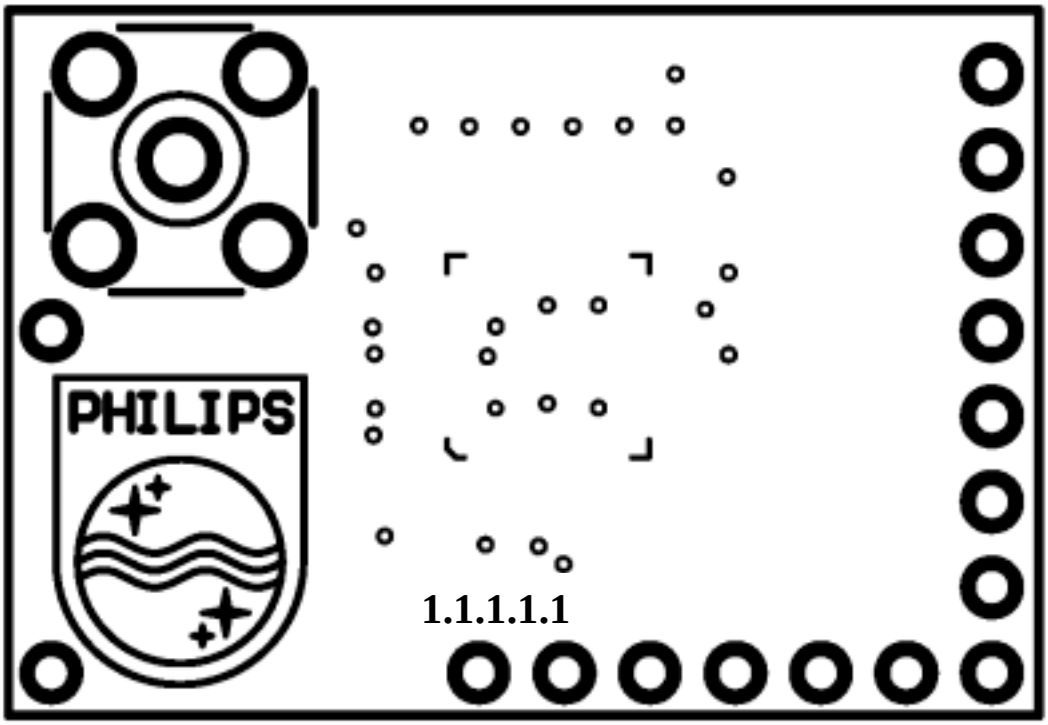


Figure A-4 REFERENCE BOTTOM TEA5767HN demo board

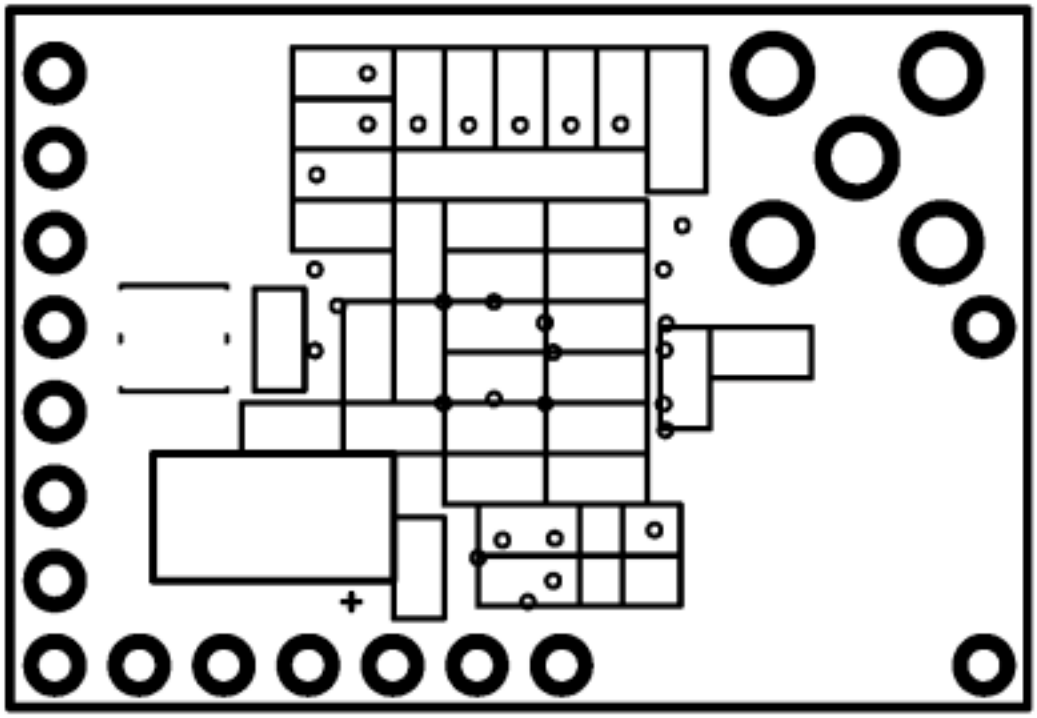


Figure A-5 SIGNAL BOTTOM TEA5767HN demo board

APPENDIX A: TEA5767HN DEMO BOARD

Item	QNT	Component	Series	Tol.	RATING	VENDOR	GEOMETRY	Refrence
1	2	100n	XR7	10%	0603	PHILIPS	C0603	C1, C2
2	2	33n	XR7	10%	0603	PHILIPS	C0603	C10, C11
3	1	1n	XR7	10%	0603	PHILIPS	C0603	C14
4	1	10p	NP0	10%	0603	PHILIPS	C0603	C15
5	1	4n7	XR7		0603	PHILIPS	C0603	C16
6	1	0pen						C17
7	1	47n	XR7	10%	0603	PHILIPS	C0603	C19
8	1	10n	XR7	10%	0603	PHILIPS	C0603	C20
9	1	100p	NP0	10%	0603	PHILIPS	C0603	C3
10	6	22n	XR7	10%	0603	PHILIPS	C0603	C4, C5,C12, C21, C22, C23
11	1	27p	NP0	10%	603	PHILIPS	C0603	C13
12	1	47p	NP0	10%	0603	PHILIPS	C0603	C6
13	3	47n	XR7	10%	0603	PHILIPS	C0603	C7, C8, C9
14	1	47uF	XR7	10%	1812	PHILIPS	C0603	CP3
15	2	BB202	VARICAP		0603	PHILIPS	C0603	D2, D3
16	1	120nH	LQW18ANR12J00	5%	0603	muRATA	C0603	L1
17	2	33nH	LQW18AN33NG00	2%	0603	muRATA	C0603	L2, L3
18	1	ANT			BNC_SUB			P1
19	1	10R	RC21	5%	0603	PHILIPS	R0603	R1
20	3	0R	RC21	5%	603	PHILIPS	R0603	R6, R22, R23
21	1	33K	RC21	5%	0603	PHILIPS	R0603	R16
22	1	10k	RC21	5%	0603	PHILIPS	R0603	R20
23	1	100k	RC21	5%	0603	PHILIPS	R0603	R21
24	1	18K	RC12G, TC50	1%	0805	PHILIPS	R0805	R25
25	2	ARRAY_1x7p	05-88-1136					
26	1	ARRAY_1x7p	05-88-1136					
27	1	IC1	HVQFN40			PHILIPS	SOT618	TEA5767HN
28	1	13MHz	NX4025			NDK		X1

Figure A-6 BOM list TEA5767HN demo board

APPENDIX B: TEA5768HL DEMO BOARD

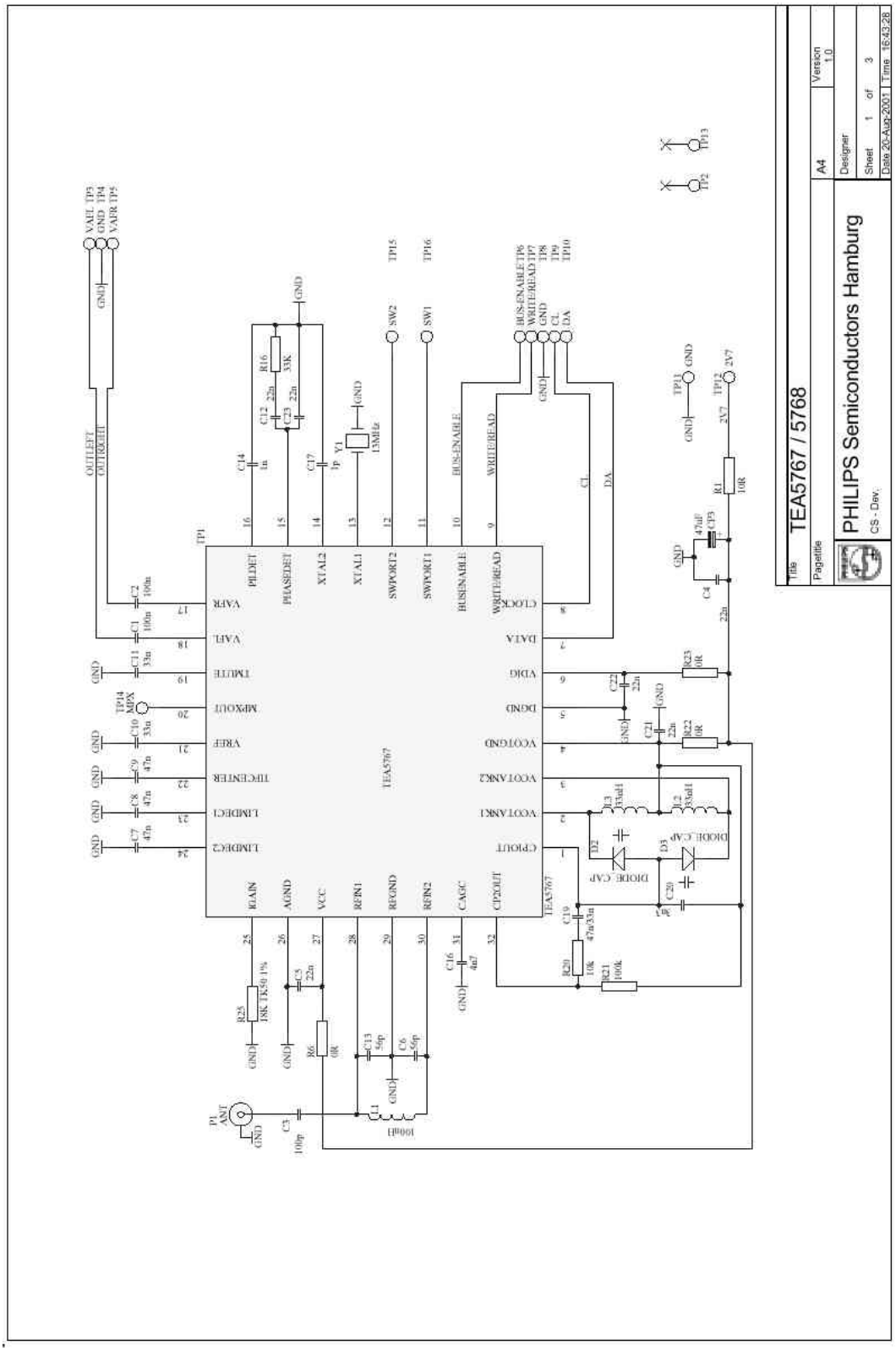


Figure B-1 SCHEMATIC TEA5767/68HL demo board

APPENDIX B: TEA5767/68HL DEMO BOARD

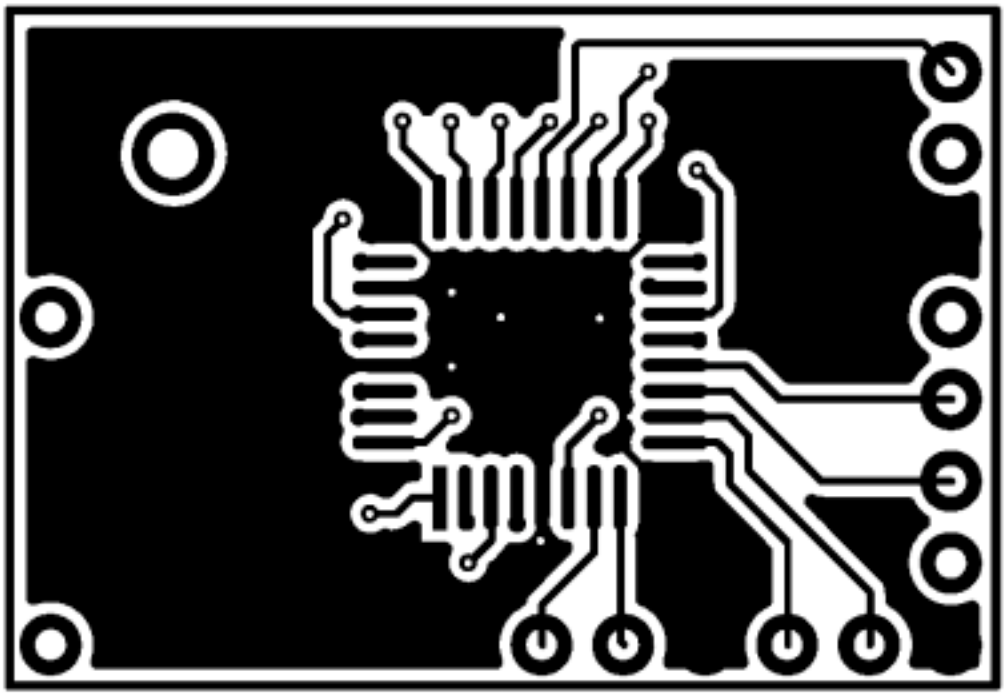


Figure B-2 REFERENCE TOP TEA5767/68HL demo board

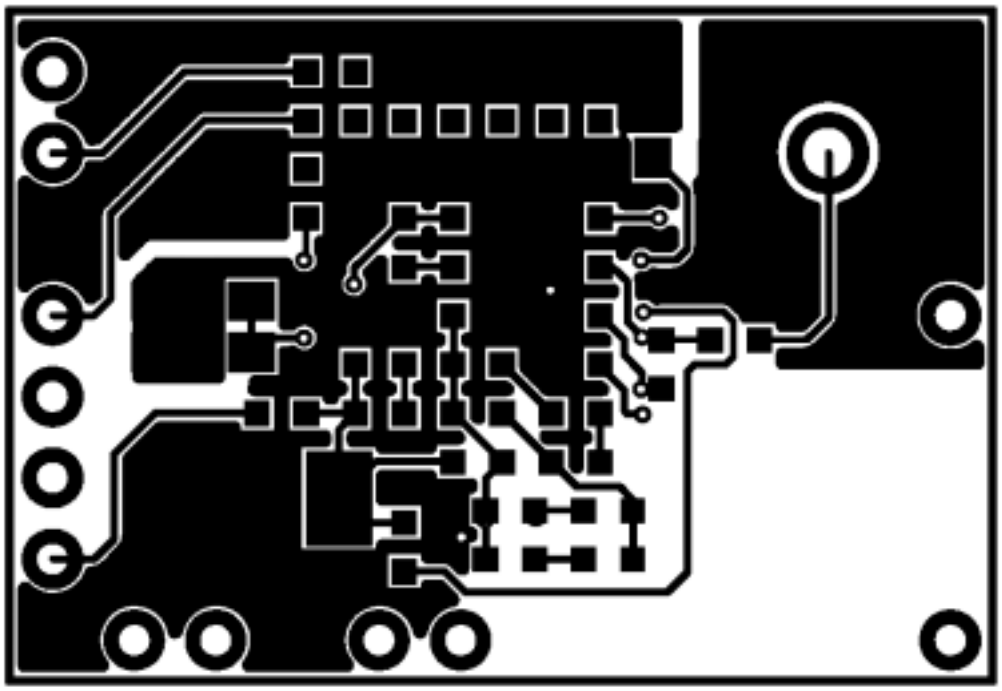


Figure B-3 SIGNAL TOP TEA5767/68HL demo board

APPENDIX B: TEA5767/68HL DEMO BOARD

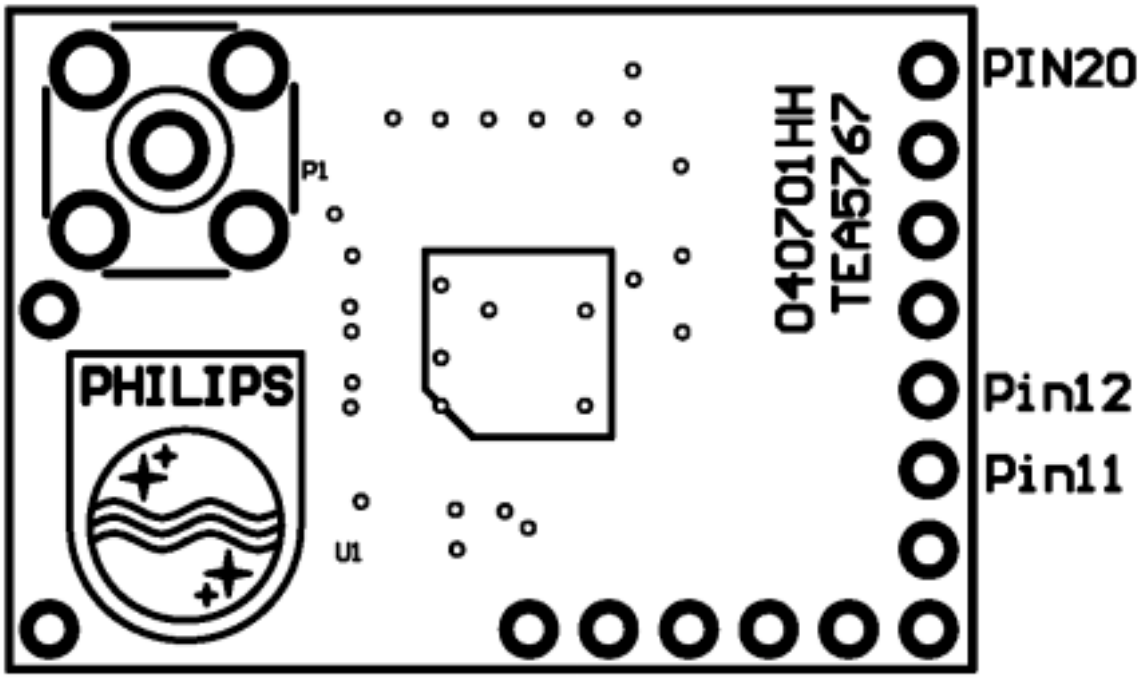


Figure B-4 REFERENCE BOTTOM TEA5767/68HL demo board

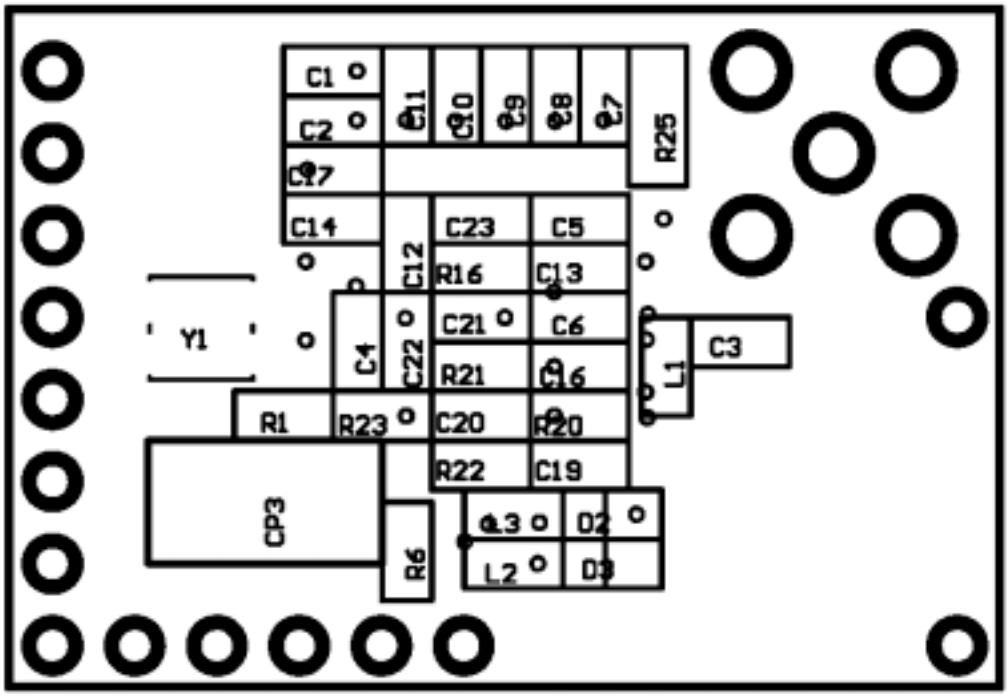


Figure B-5 SIGNAL BOTTOM TEA5767/68HL demo board

APPENDIX B: TEA5767/68HL DEMO BOARD

Item	QNT	Component	Series	Tol.	RATING	VENDOR	GEOMETRY	Refrence
1	2	100n	XR7	10%	0603	PHILIPS	C0603	C1, C2
2	2	33n	XR7	10%	0603	PHILIPS	C0603	C10, C11
3	1	1n	XR7	10%	0603	PHILIPS	C0603	C14
4	1	10p	NP0	10%	0603	PHILIPS	C0603	C15
5	1	4n7	XR7		0603	PHILIPS	C0603	C16
6	1	1p	NP0	10%	606	PHILIPS	C0603	C17
7	1	47n	XR7	10%	0603	PHILIPS	C0603	C19
8	1	10n	XR7	10%	0603	PHILIPS	C0603	C20
9	1	100p	NP0	10%	0603	PHILIPS	C0603	C3
10	6	22n	XR7	10%	0603	PHILIPS	C0603	C4, C5,C12, C21, C22, C23
11	1	27p	NP0	10%	603	PHILIPS	C0603	C13
12	1	47p	NP0	10%	0603	PHILIPS	C0603	C6
13	3	47n	XR7	10%	0603	PHILIPS	C0603	C7, C8, C9
14	1	47uF	XR7	10%	1812	PHILIPS	C0603	CP3
15	2	BB202	VARICAP		0603	PHILIPS	C0603	D2, D3
16	1	120nH	LQW18ANR12J00	5%	0603	muRATA	C0603	L1
17	2	33nH	LQW18AN33NG00	2%	0603	muRATA	C0603	L2, L3
18	1	ANT			BNC_SUB			P1
19	1	10R	RC21	5%	0603	PHILIPS	R0603	R1
20	3	0R	RC21	5%	603	PHILIPS	R0603	R6, R22, R23
21	1	33K	RC21	5%	0603	PHILIPS	R0603	R16
22	1	10k	RC21	5%	0603	PHILIPS	R0603	R20
23	1	100k	RC21	5%	0603	PHILIPS	R0603	R21
24	1	18K	RC12G, TC50	1%	0805	PHILIPS	R0805	R25
25	2	ARRAY_1x7p	05-88-1136					
26	1	ARRAY_1x5p	05-88-1136					
27	1	IC1	LQFP32			PHILIPS	SOT358	TEA5768HL
28	1	13MHz	NX4025			NDK		X1

Figure B-6 BOM list TEA5767/68HL demo board

APPENDIX C: PR37002 MOTHER BOARD (WITH TDA7053AT AND SAA6588T)

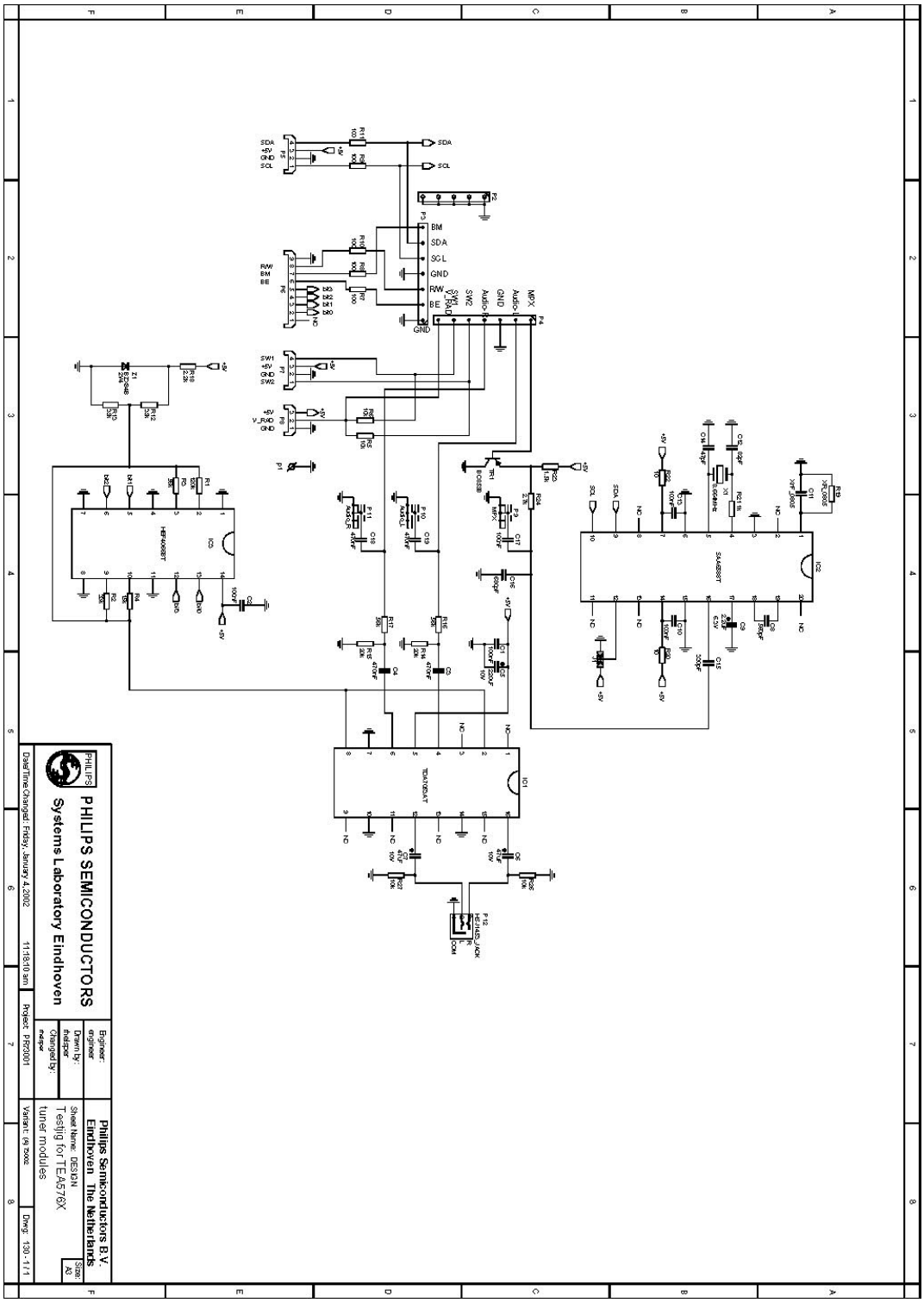


Figure C: schematic diagram of PR73002 mother board

APPENDIX D: PR37156 DSM INTERFACE

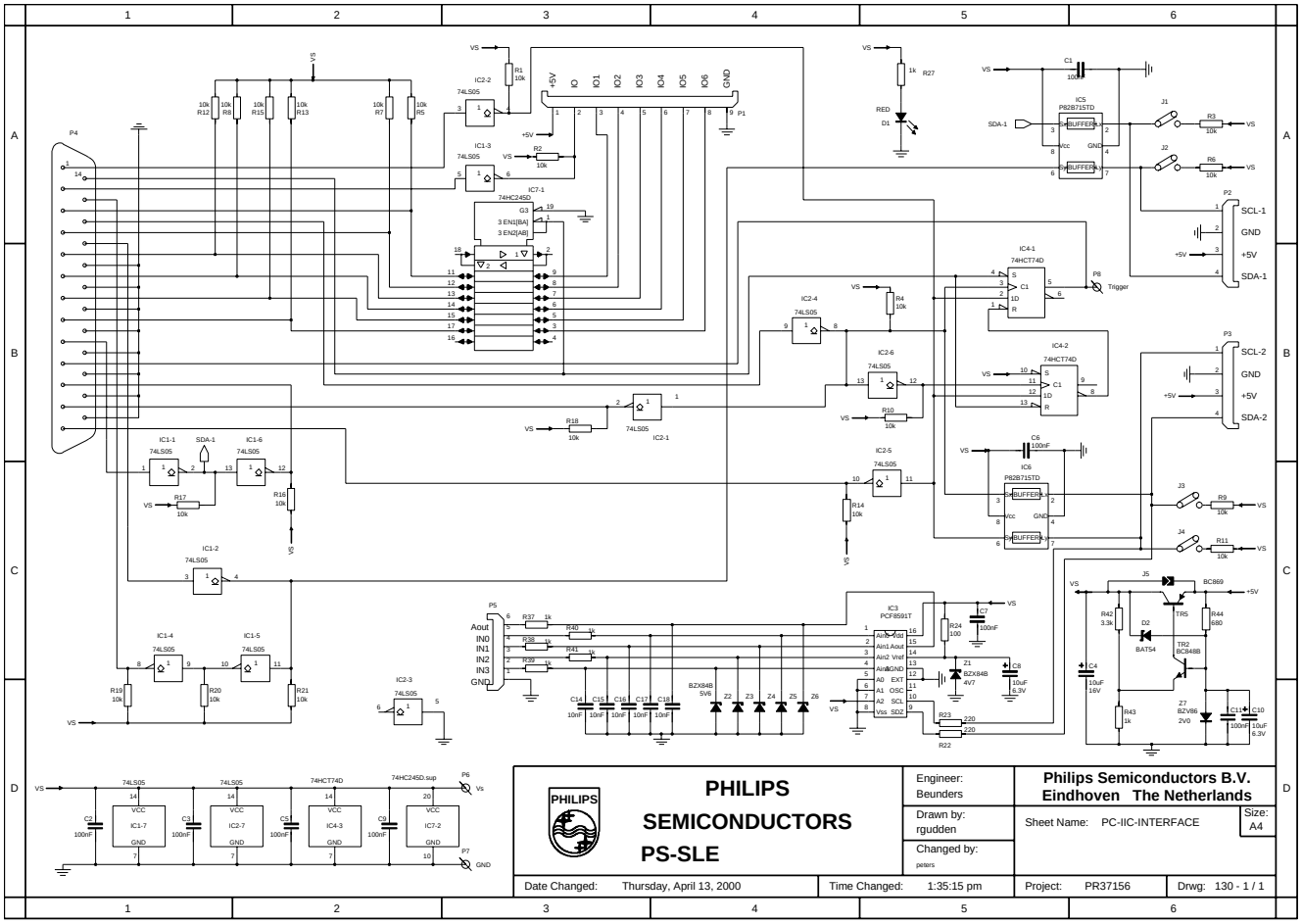


Figure D: schematic diagram PR37156 DSM (Dual Single Master) interface

APPENDIX E: COMMUNICATION: WRITE MODE

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data byte 1	mute	Search mode	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8
Data byte 2	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
Data byte 3	Search up/down	Search stop level		HiLo side injection	Mono/stereo	Mute left	Mute right	SW port1
Data byte 4	SW port 2	Stand-by	Band limits	xtal	Soft-mute	HCC	SNC	Search indicator
Data byte 5	PLL ref	Deemph	Not used	Not used	Not used	Not used	Not used	Not used

Data	**Description**
Mute	1: L-, R-audio muted 0: Audio not muted
Search node	1: search mode 0: not in search mode
PLL13..PLL0	Setting of the synthesizer programmable counter
Search up/down	1: search up 0: search down
Search stop level	See table 4 (page 29)
High/low side injection	1: high side LO injection 0: low side LO injection
Mono/stereo	1: forced mono 0: stereo on
Mute left	1: left audio muted and forced mono 0: not muted
Right mute	1: Right audio muted and forced mono 0: not muted
SW port 1 & SW port 2	1: Port high 0: Port low
Stand-by	1: tuner in stand-by 0: not in stand-by
Band limits (BL)	1: japan FM band US/Europe FM band
Xtal	1: Fxtal is 32.768kHz 0: Fxtal is 13MHz
Soft_mute	1: On 0: Off
HCC	1: On 0: Off
SNC	1: On 0: Off
Search indicator	1: pin 14 is output for the ready flag 0: pin 14 is SW port 1
PLL ref	1: 6.5MHz reference for PLL enabled 0: 6.5MHz reference not enabled
Deemph	1: deemphasis time constant is 75us 0: deemphasis time constant is 50us

APPENDIX F: COMMUNICATION: READE MODE

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data byte 1	Ready flag	Band limit flag	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8
Data byte 2	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
Data byte 3	Stereo indication	IF6	IF5	IF4	IF3	IF2	IF1	IF0
Data byte 4	LEV3	LEV2	LEV1	LEV0	Chip ID2	Chip ID1	Chip ID0	Not used
Data byte 5	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	Reserve

Data	**Description**
Ready flag	1: Tuning completed or BL reached 0: Busy
Band limit flag	1: Band limit reached 0: Band limit not reached
PLL13…PLL0	Setting of the synthesizer programmable counter
Stereo indication	1: Stereo reception 0: Mono reception
IF6…IF0	IF counter result
LEV3…LEV0	Level ADC output